

# MS-G019

Ver: 10

mini-ITX : 192 \* 180 mm

## SOC:

Intel - Braswell M/D

## OnBoard Chipset:

AUDIO:REALTEK/ALC662-VD0

LAN:REALTEK/RTL8111G-CG

SIO:NUVOTON/NCT6793D

Flash ROM: 64Mb SPI (SOC)

## Main Memory:

DDRIII L SO-DIMM(1066/1333MHz) \* 2 (Dual Channel)

## Expansion Slots:

PCI Express (X16) Slot\*1

Mini-PCIe connector\*1

## PWM:

VCCP:ON Semiconductor/NCP81201MNTXG

VGG:ON Semiconductor/NCP81201MNTXG

VNN:TI/TPS51211DSCR

DDR:TI/TPS51216RUKR

STSTEM:TI/TPS51225CRUKR

## Other:

SATA2.0 x2

USB2.0 RearX4 Front X2

USB3.0 RearX4

DP to D-SUB\*1/HDMI\*1


LPT Header \*1

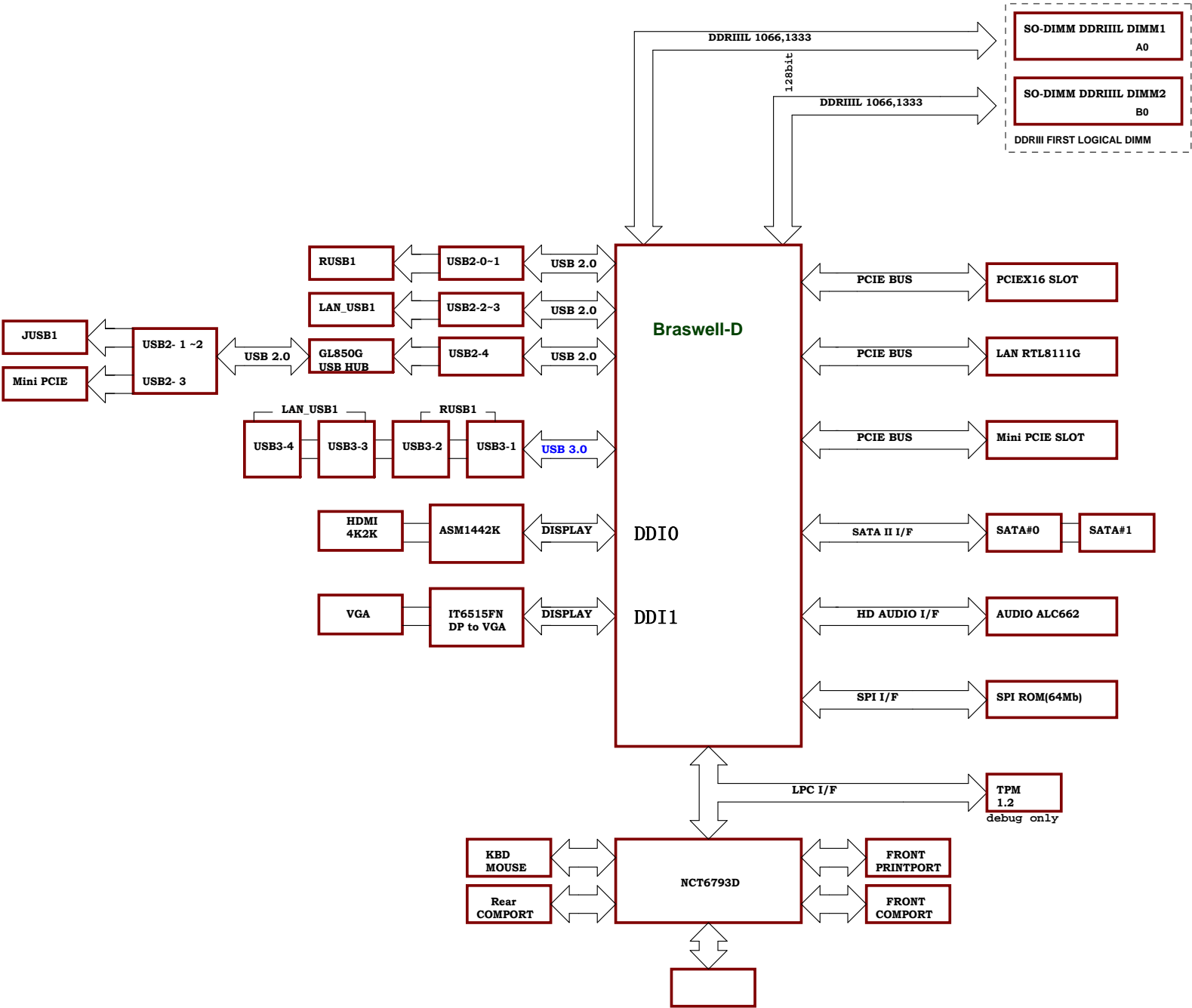
Rear COMPORT \*1

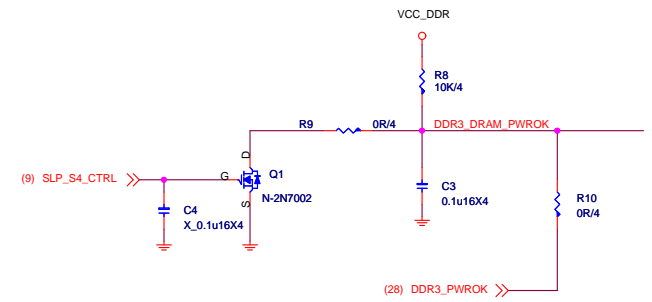
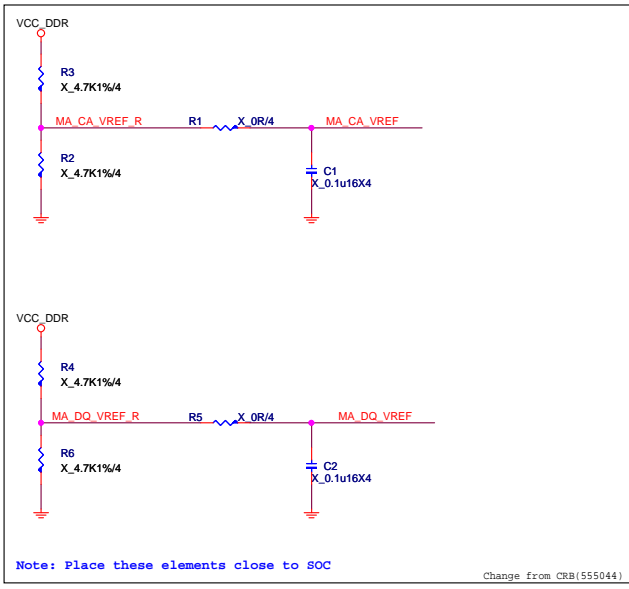
Front COMPORT \*1

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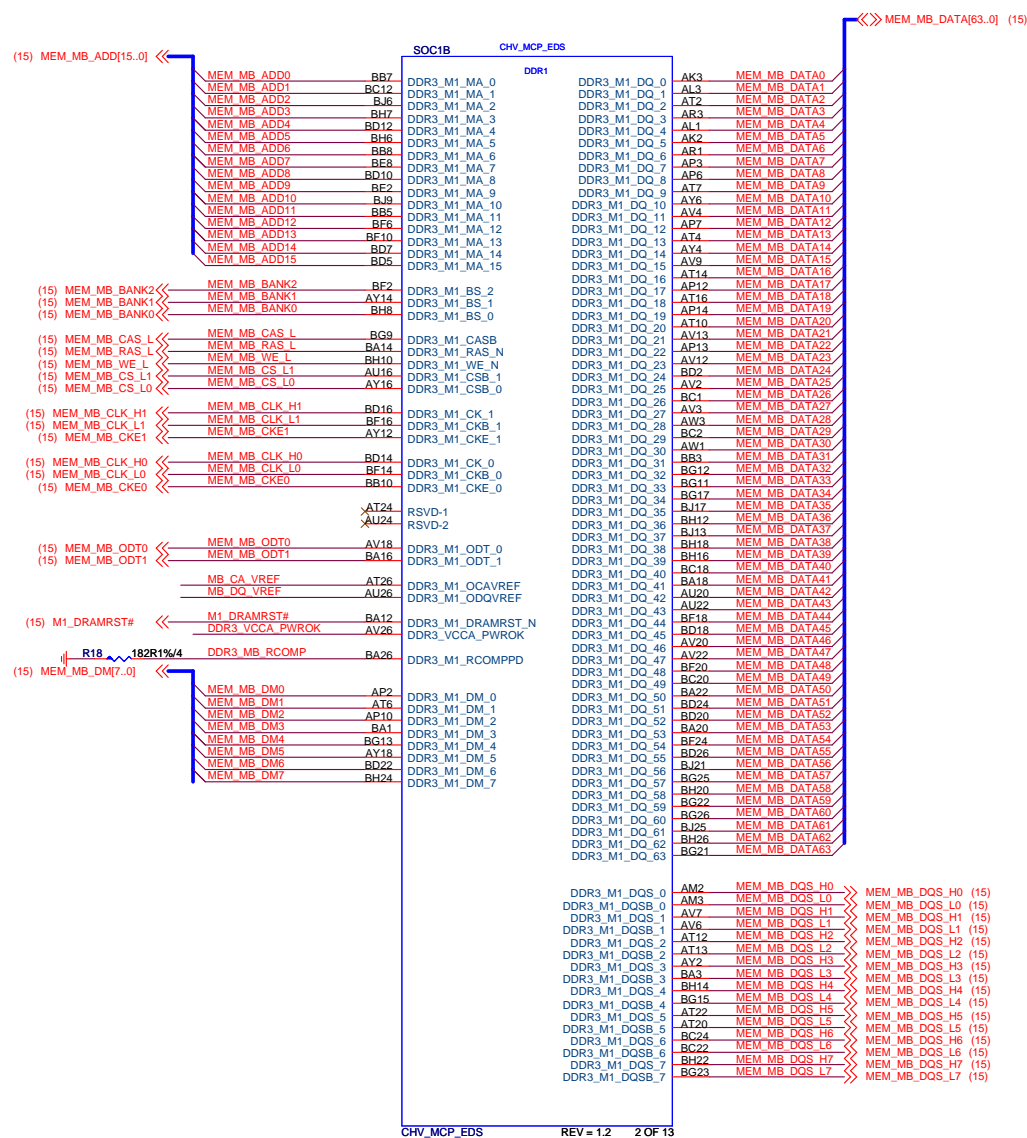
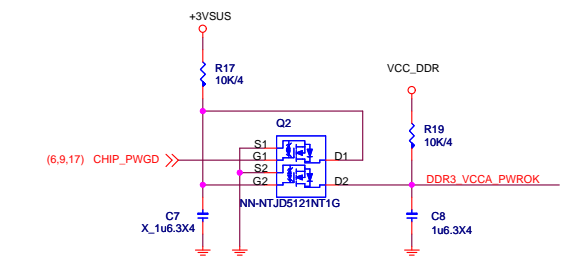
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	Mini-ITX Intel Braswell N3150 QS,2DDR3L SO-DIMM, PCI_E*16*1,Mini-PCI_E*1,ALC662-VD, Lan RTL8111G-CG, SATA3.0*2, HDMI*1,D_Sub*1	CFG-G019-020	601-G019-	A

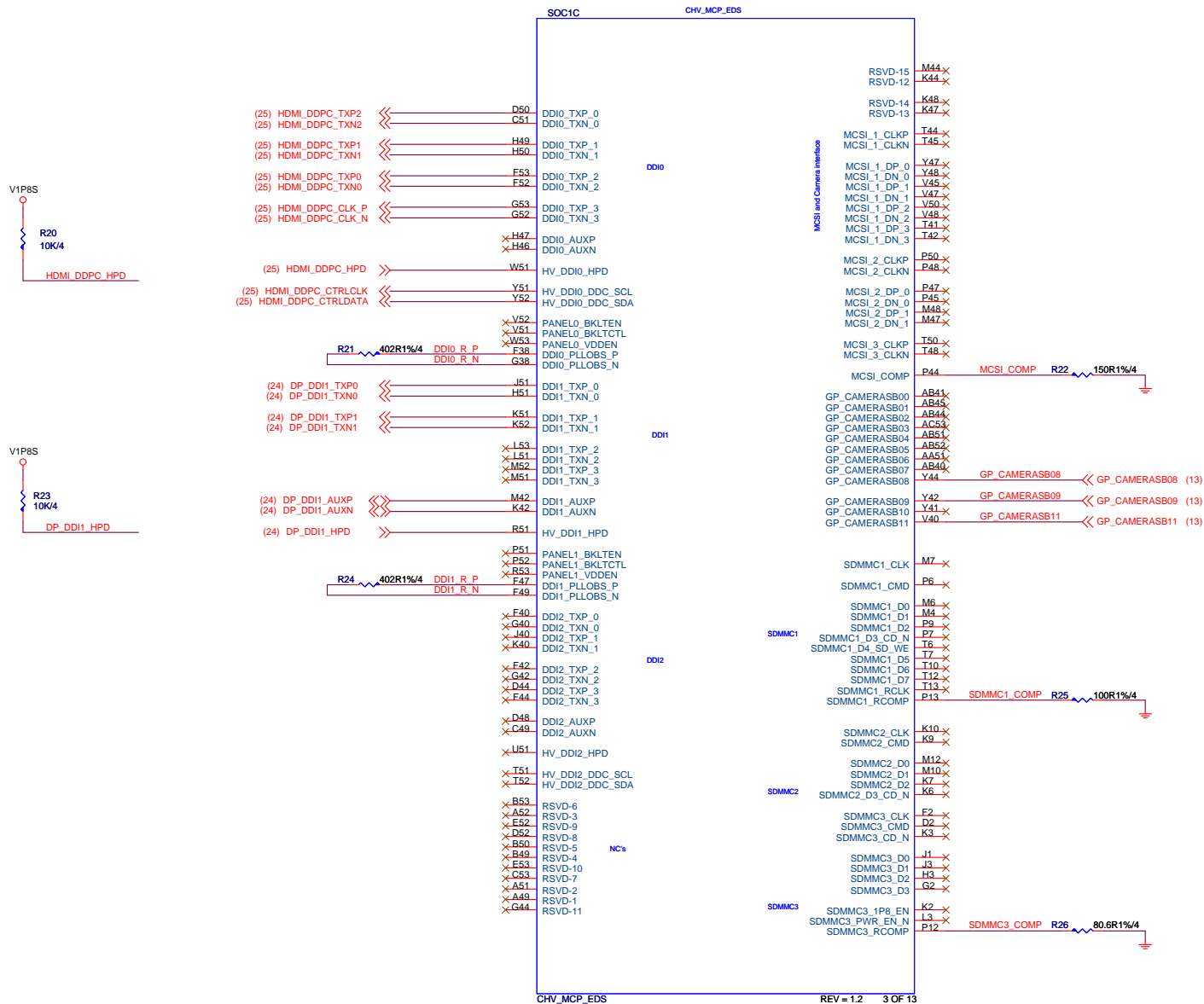
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Title <b>MS-G019</b>			
Size	Document Number		Rev
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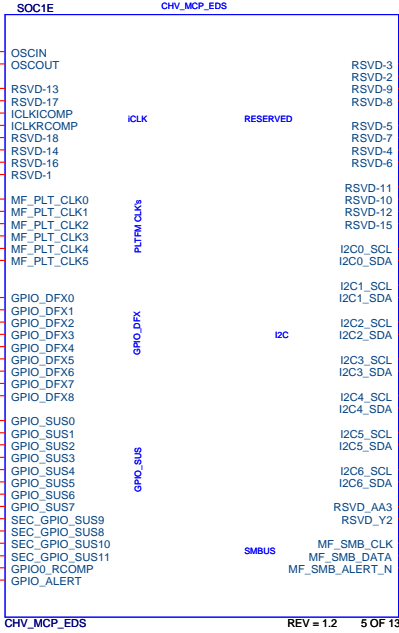
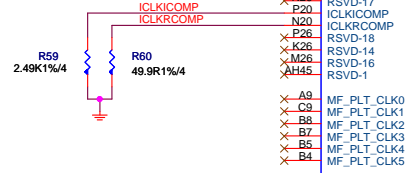
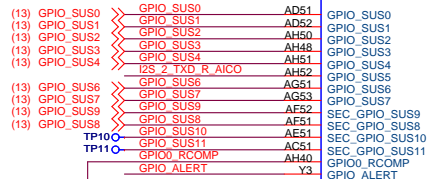
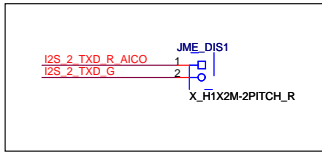
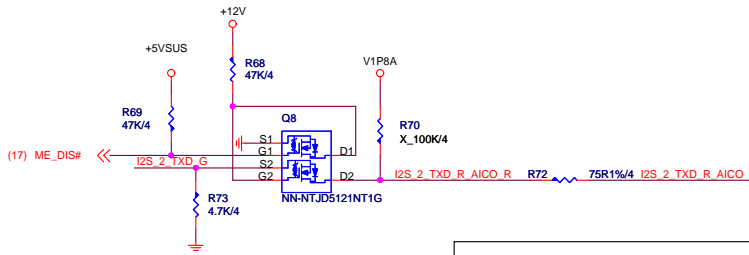
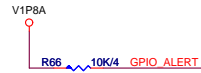
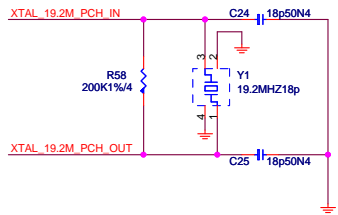


		SOC1A		CHV_MCP_EDS				MEM_MA_DATA[63..0] (14)	
(14) MEM_MA_ADD[15..0]				DORO					
		MEM MA ADD0	BB47	DDR3_M0_MA_0		AK51	MEM MA DATA0		
		MEM MA ADD1	BC42	DDR3_M0_MA_1		AL51	MEM MA DATA1		
		MEM MA ADD2	BJ48	DDR3_M0_MA_2		AT52	MEM MA DATA2		
		MEM MA ADD3	BH47	DDR3_M0_MA_3		AR51	MEM MA DATA3		
		MEM MA ADD4	BD42	DDR3_M0_MA_4		AL53	MEM MA DATA4		
		MEM MA ADD5	BH48	DDR3_M0_MA_5		AK52	MEM MA DATA5		
		MEM MA ADD6	BE46	DDR3_M0_MA_6		AR53	MEM MA DATA6		
		MEM MA ADD7	BE46	DDR3_M0_MA_7		AP51	MEM MA DATA7		
		MEM MA ADD8	BD44	DDR3_M0_MA_8		AP48	MEM MA DATA8		
		MEM MA ADD9	BE52	DDR3_M0_MA_9		AT47	MEM MA DATA9		
		MEM MA ADD10	BJ45	DDR3_M0_MA_10		AY48	MEM MA DATA10		
		MEM MA ADD11	BE40	DDR3_M0_MA_11		AV50	MEM MA DATA11		
		MEM MA ADD12	BF48	DDR3_M0_MA_12		AP47	MEM MA DATA12		
		MEM MA ADD13	BF44	DDR3_M0_MA_13		AT50	MEM MA DATA13		
		MEM MA ADD14	BD47	DDR3_M0_MA_14		AY50	MEM MA DATA14		
		MEM MA ADD15	BD49	DDR3_M0_MA_15		AV45	MEM MA DATA15		
				DDR3_M0_BS_2		AT40	MEM MA DATA16		
(14) MEM_MA_BANK2		MEM MA BANK2	BF52	DDR3_M0_BS_1		AP42	MEM MA DATA17		
(14) MEM_MA_BANK1		MEM MA BANK1	AY40	DDR3_M0_BS_0		AT38	MEM MA DATA18		
(14) MEM_MA_BANK0		MEM MA BANK0	BH46			AP40	MEM MA DATA19		
				DDR3_M0_CAS_N		AT44	MEM MA DATA20		
(14) MEM_MA_CAS_L		MEM MA CAS_L	BG45	DDR3_M0_RAS_N		AV41	MEM MA DATA21		
(14) MEM_MA_RAS_L		MEM MA RAS_L	BA40	DDR3_M0_WE_N		AP41	MEM MA DATA22		
(14) MEM_MA_WE_L		MEM MA WE_L	BH44	DDR3_M0_CSB_1		AV42	MEM MA DATA23		
(14) MEM_MA_CS_L1		MEM MA CS_L1	AY38	DDR3_M0_CSB_0		BD52	MEM MA DATA24		
(14) MEM_MA_CS_L0		MEM MA CS_L0	AY38			AV52	MEM MA DATA25		
				DDR3_M0_CLK_1		BC53	MEM MA DATA26		
(14) MEM_MA_CLK_H1		MEM MA CLK_H1	BD38	DDR3_M0_CK_1		AV51	MEM MA DATA27		
(14) MEM_MA_CLK_L1		MEM MA CLK_L1	BF38	DDR3_M0_CKB_1		AW51	MEM MA DATA28		
(14) MEM_MA_CKE1		MEM MA CKE1	AY42	DDR3_M0_CKB_0		BC52	MEM MA DATA29		
				DDR3_M0_CK_0		AW53	MEM MA DATA30		
(14) MEM_MA_CLK_H0		MEM MA CLK_H0	BD40	DDR3_M0_CK_0		BB51	MEM MA DATA31		
(14) MEM_MA_CLK_L0		MEM MA CLK_L0	BF40	DDR3_M0_CKB_0		BG42	MEM MA DATA32		
(14) MEM_MA_CKE0		MEM MA CKE0	BD44	DDR3_M0_CKE_0		BG43	MEM MA DATA33		
				RSVD-1		BG37	MEM MA DATA34		
				RSVD-2		BJ37	MEM MA DATA35		
						BH42	MEM MA DATA36		
(14) MEM_MA_ODT0		MEM MA ODT0	AV36	DDR3_M0_ODT_0		BJ41	MEM MA DATA37		
(14) MEM_MA_ODT1		MEM MA ODT1	BA38	DDR3_M0_ODT_1		BH36	MEM MA DATA38		
		MA CA VREF		DDR3_M0_ODT_2		BH38	MEM MA DATA39		
		MA DQ VREF	AT28	DDR3_M0_OCAVREF		BC36	MEM MA DATA40		
			AU28	DDR3_M0_ODQVREF		BA36	MEM MA DATA41		
(14) M0_DRAMRST#		M0_DRAMRST#	BA42	DDR3_M0_DRAMRST_N		AU34	MEM MA DATA42		
		DDR3_DRAM_PWROK	BA28	DDR3_DRAM_PWROK		AU32	MEM MA DATA43		
				DDR3_M0_RCOMP		BF36	MEM MA DATA44		
(14) MEM_MA_DM[7..0]						BD36	MEM MA DATA45		
						AV34	MEM MA DATA46		
						AV32	MEM MA DATA47		
						BF34	MEM MA DATA48		
						BC34	MEM MA DATA49		
						BA32	MEM MA DATA50		
						BD30	MEM MA DATA51		
						BD34	MEM MA DATA52		
						BA34	MEM MA DATA53		
						BF30	MEM MA DATA54		
						BD28	MEM MA DATA55		
						BI33	MEM MA DATA56		
						BG29	MEM MA DATA57		
						BH34	MEM MA DATA58		
						BG32	MEM MA DATA59		
						BG28	MEM MA DATA60		
						BJ29	MEM MA DATA61		
						BH28	MEM MA DATA62		
						BG33	MEM MA DATA63		

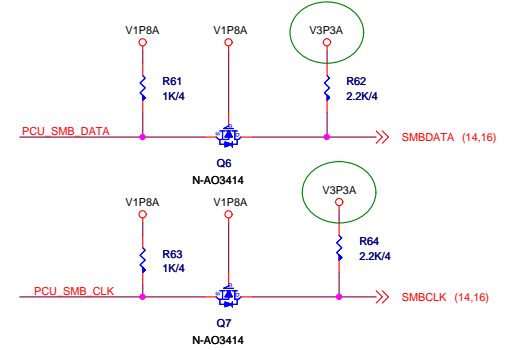




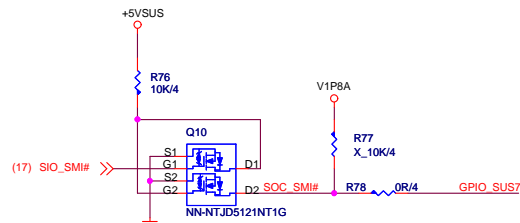
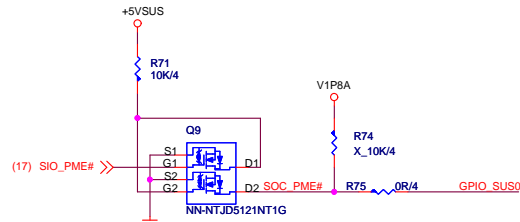


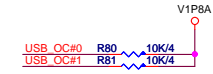
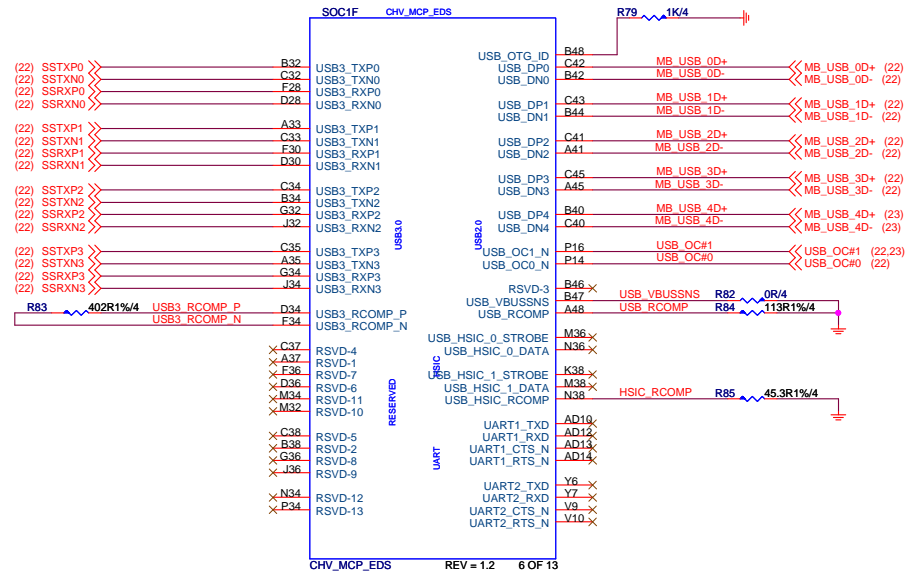


Q6/Q7Vgs<1V.

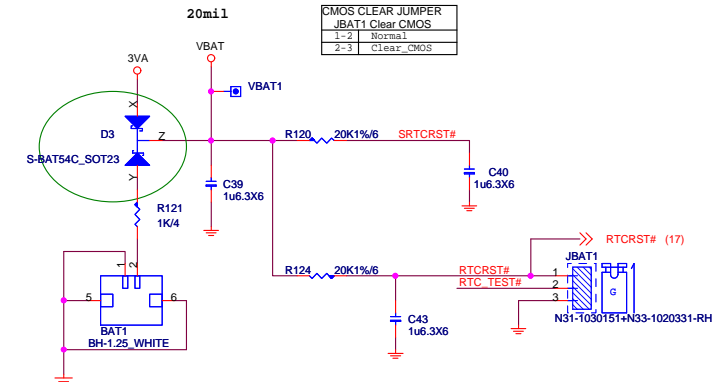
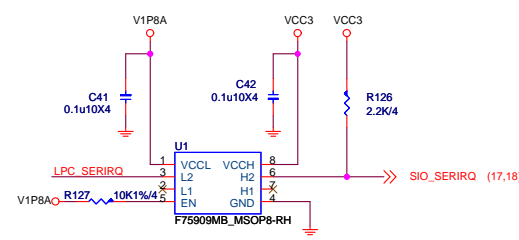
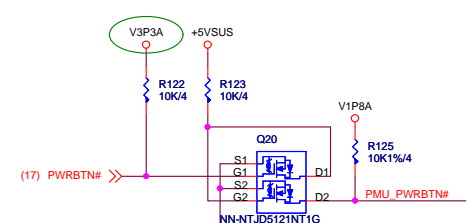
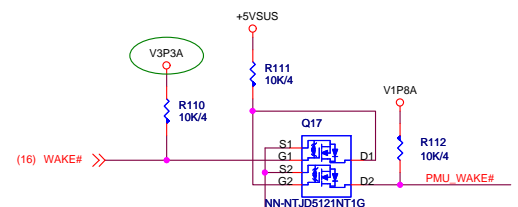
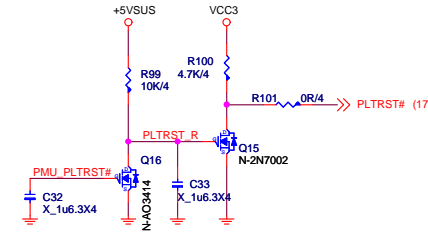
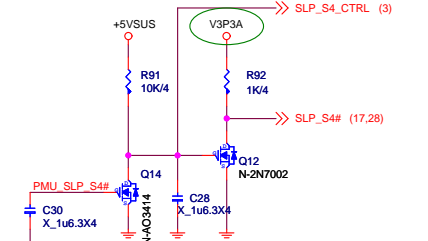


## PMC Level shift



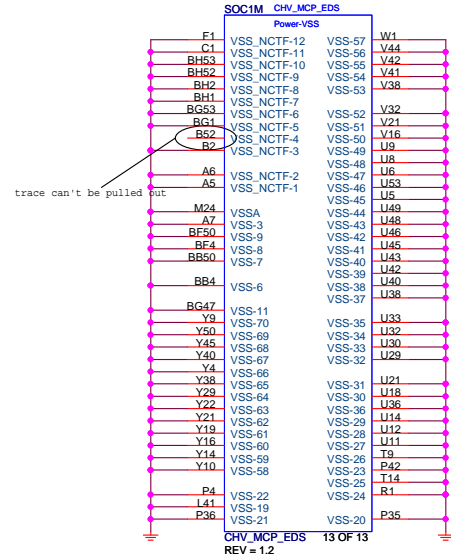
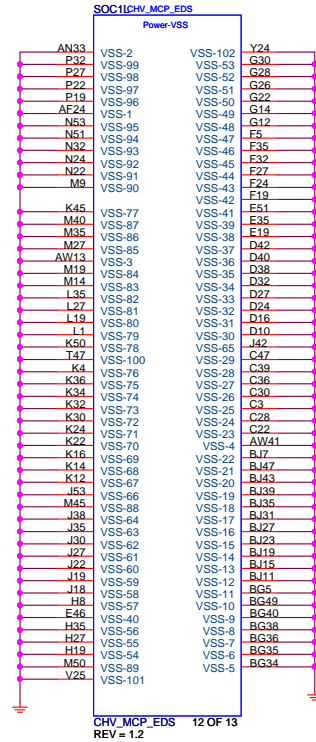
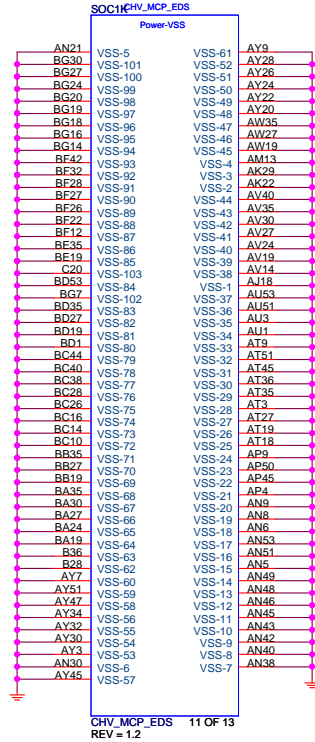
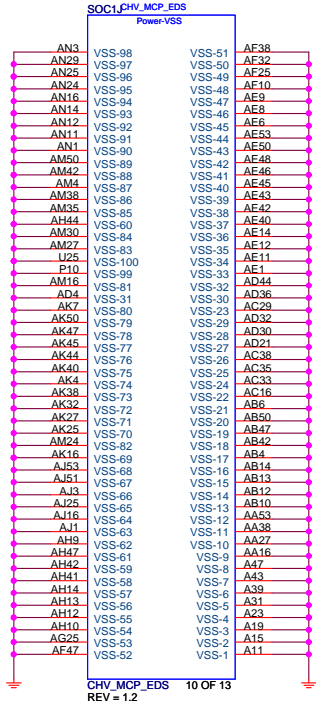












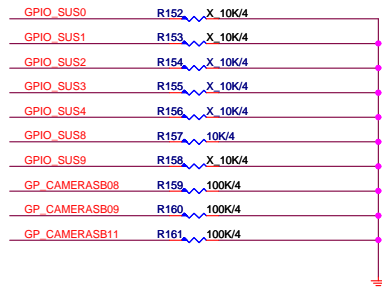
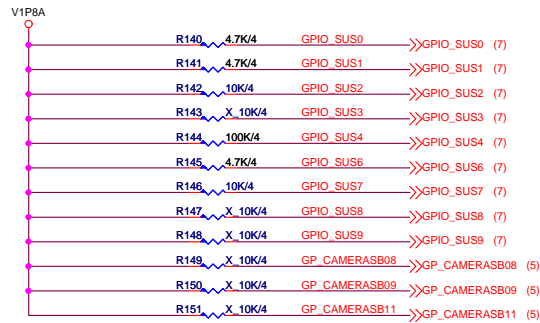


Table 24-1. Digital Display Ports Enable and Disable Guidelines

Port	Strap	How to Enable Port	How to Disable Port
DDI0	GPIO_SUS0	Pull-up to V1P8A with 4.7-K $\Omega$ $\pm$ 5% resistor	N/A, Weak internal pull-down
DDI1	GPIO_SUS1	Pull-up to V1P8A with 4.7-K $\Omega$ $\pm$ 5% resistor	N/A, Weak internal pull-down

**Note:** DDI2 is always enabled an no Hard Strap is needed.

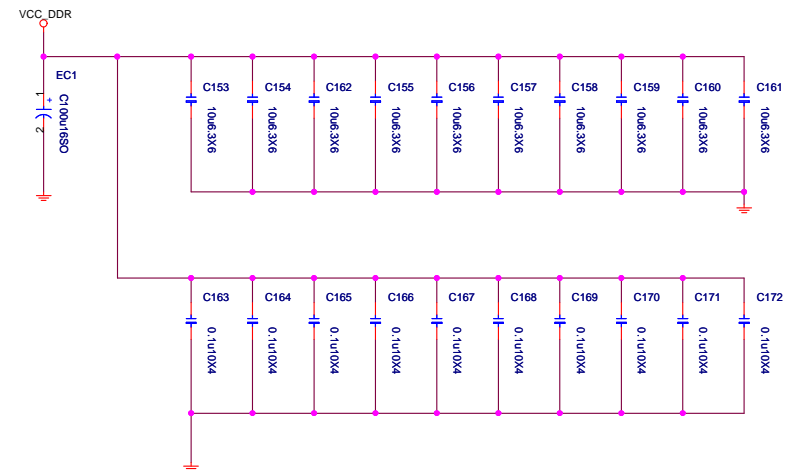
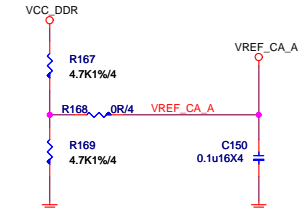
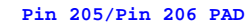
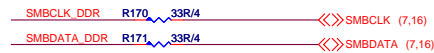
Table 2-26. Hard Strap Description and Functionality (Sheet 1 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal (20k PD)	0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal (20k PD)	0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	Top Swap (A16) override	Weak internal (20k PU)	0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[3]	MIPI-DSI Display Detect	Weak internal (20k PD)	0 = DSI Port not detected 1 = DSI Port detected <b>Note:</b> DSI is not POR for BSW. This strap will not enable DSI on BSW. Leave the pin floating if GPIO functionality is not used.
GPIO_SUS[4]	Boot BIOS Strap (BBS)	Weak internal (20k PU)	0 = No SPI (Default) 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal (20k PU)	0 = Not supported 1 = Normal Operation
GPIO_SUS[6]	Halt Boot Strap	Weak internal (20k PU)	1 = Normal Operation <b>Note:</b> This strap <b>MUST</b> be High at RSMRST_N de-assert to ensure proper platform operation and use of GPIO_DFX[8:0]
GPIO_SUS[8]	PLLs, ICLK, USB2, DDI SFR Supply Select	Weak internal (20k PU)	0 = Supply is 1.25V 1 = Supply is 1.35V
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal (20k PD)	0 = No bypass 1 = Bypass with 1.05V

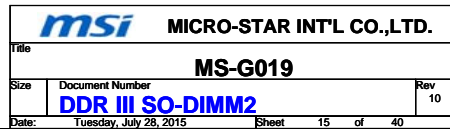
Table 2-26. Hard Strap Description and Functionality (Sheet 2 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass

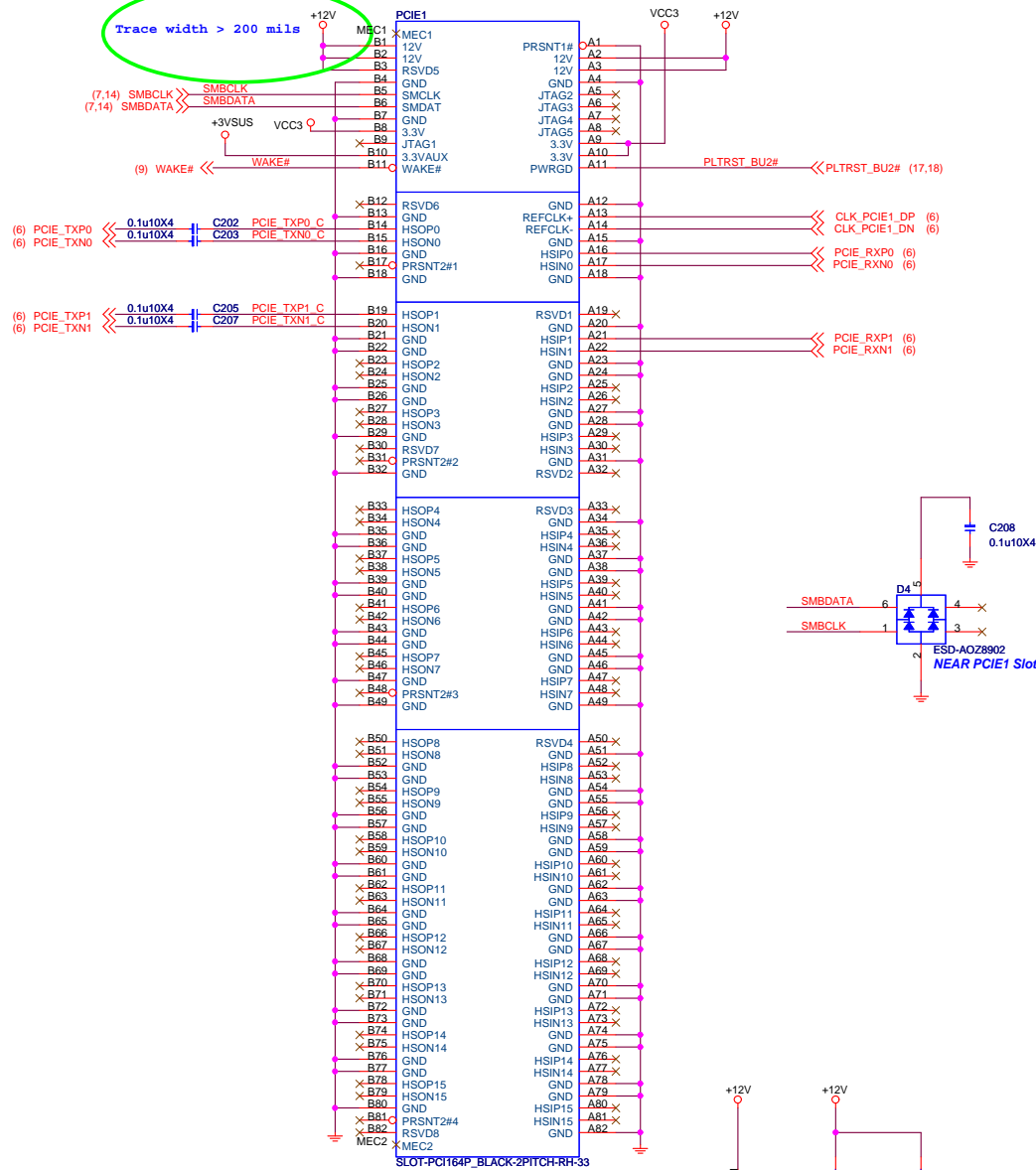
-(STD) N13-2040930-CK3 9.2H



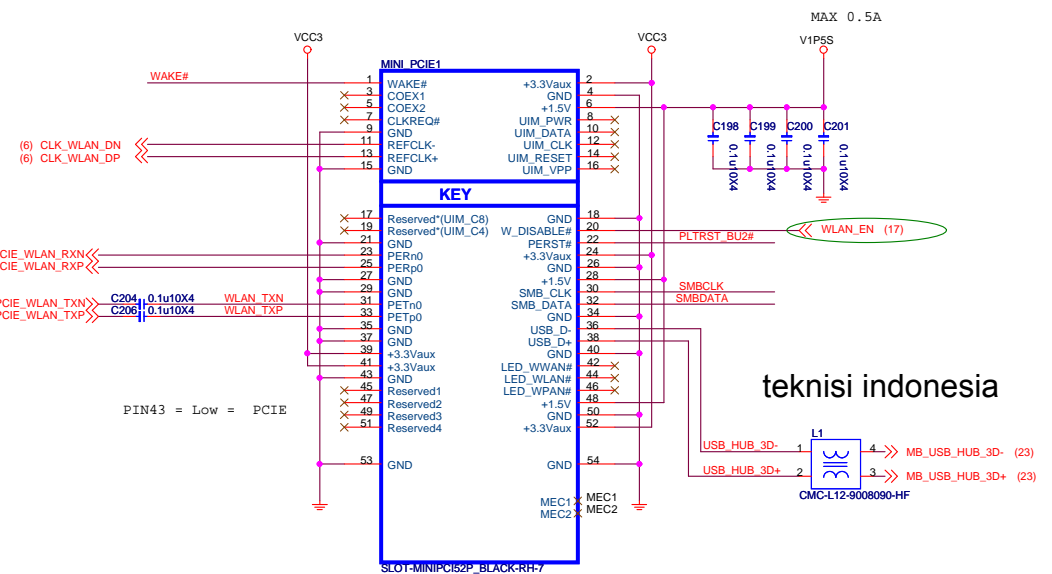
N13-2041200-CK3 9.2H



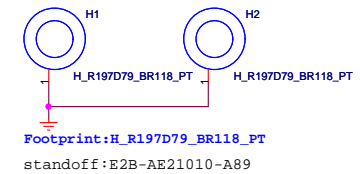
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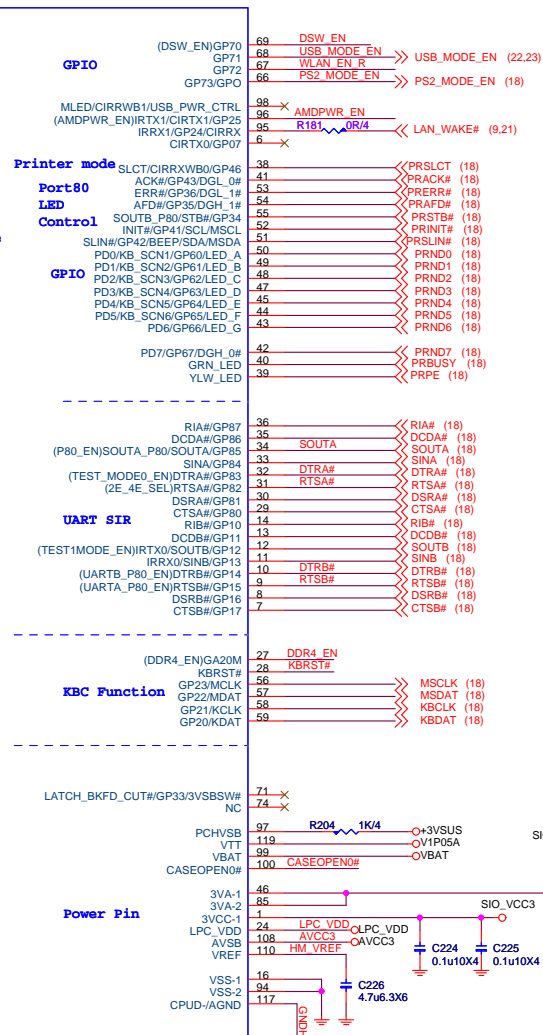
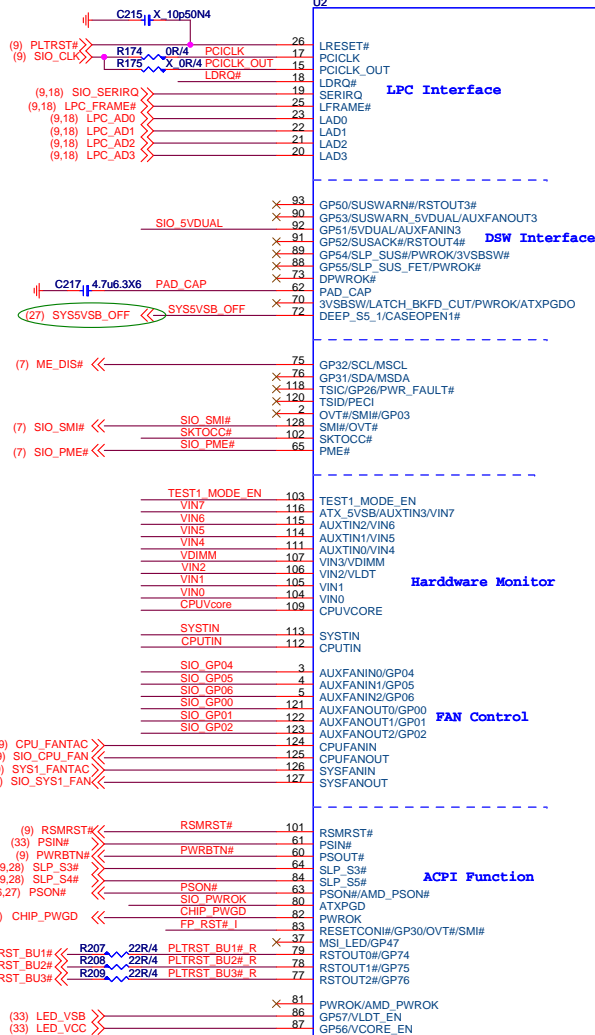
## Mini-PCIEX1



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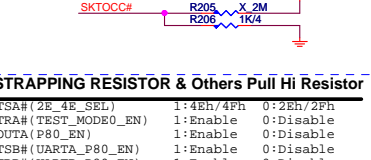
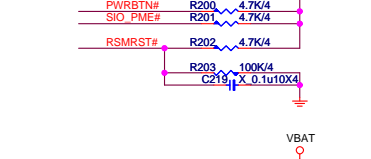
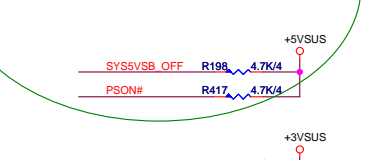
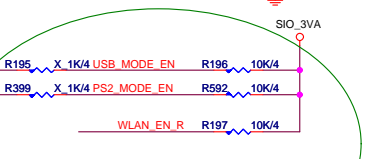
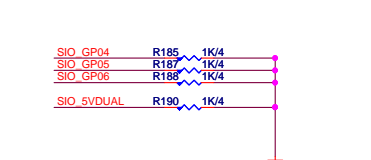
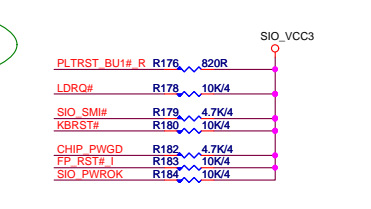
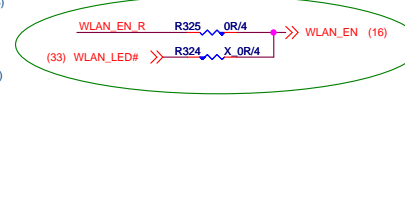




USB\_MODE\_EN(Default:GPI/VSB)  
BIOS set  
S4/S5 : GPO/OD/L  
S0/S3 : GPO/PP/H

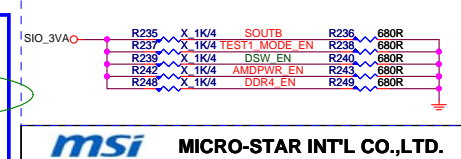
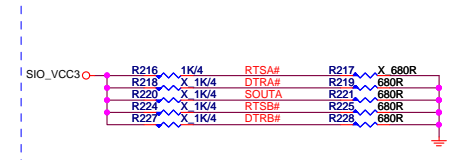
PS2\_MODE\_EN(Default:GPI/VSB)  
BIOS set  
S4/S5 : GPO/OD/L  
S0/S3 : GPO/PP/H

WLAN\_EN\_R(Default:GPI/VSB)  
BIOS set  
S4/S5 : GPO/OD/L  
S0/S3 : GPO/PP/H



### LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

FIN31	RTSA# (2E_4E_SEL)	1:4Eh/4Fh	0:2Eh/2Fh
FIN32	DTRA# (TEST_MODE0_EN)	1:Enable	0:Disable
FIN34	SOUTA (P80_EN)	1:Enable	0:Disable
FIN9	RTSB# (UARTA_P80_EN)	1:Enable	0:Disable
FIN10	DTRB# (UARTB_P80_EN)	1:Enable	0:Disable
FIN12	SOUTB (STRP_KEY_LOCK)	1:Enable	0:Disable
FIN103	TEST_MODE1_EN	1:Enable	0:Disable
FIN69	DSW_EN (DSW_EN)	1:Enable	0:Disable
FIN96	AMPDWR_EN (AMPDWR_EN)	1:Enable	0:Disable
FIN27	DDR4_EN (DDR4_EN)	1:Enable	0:Disable



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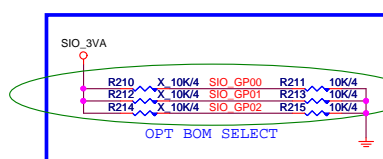
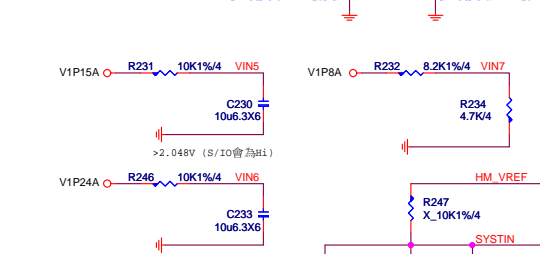
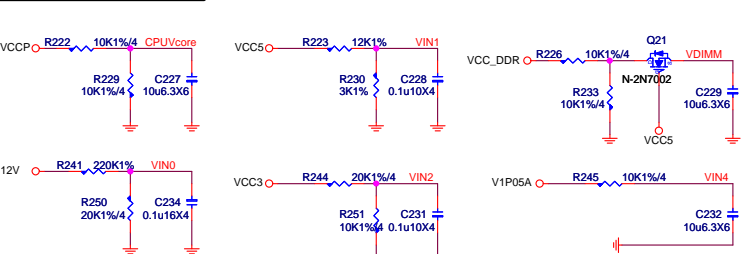
Title MS-G019

Size Document Number

Date: Tuesday, July 28, 2015 Sheet 17 of 40

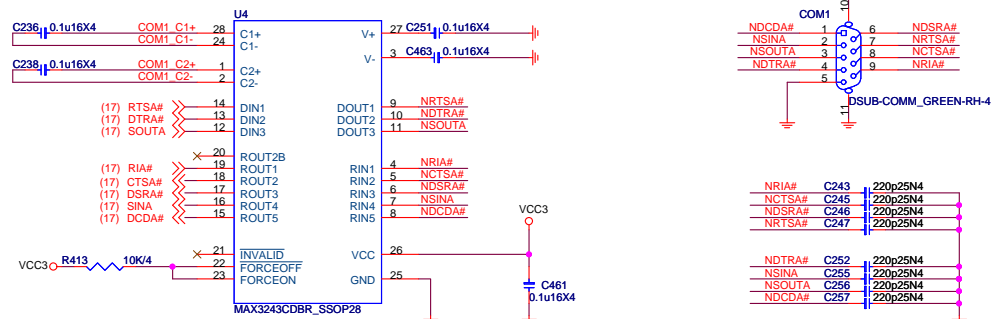
Rev 10

### HW Monitor - Voltage

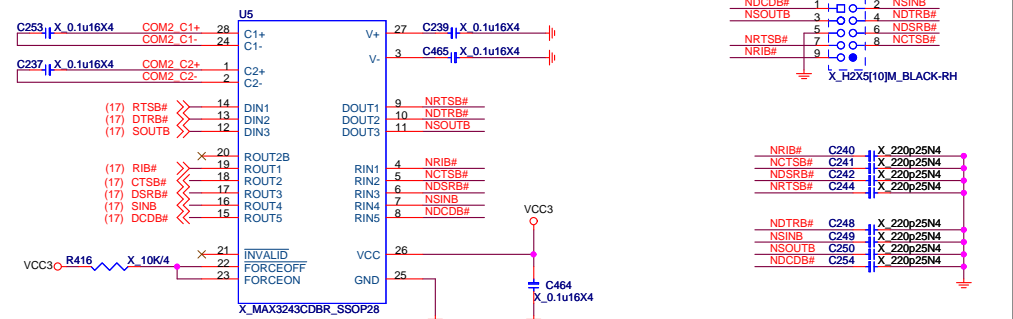


GP0	GP1	GP2
0	0	0
0	0	1

## SERIAL PORT 1

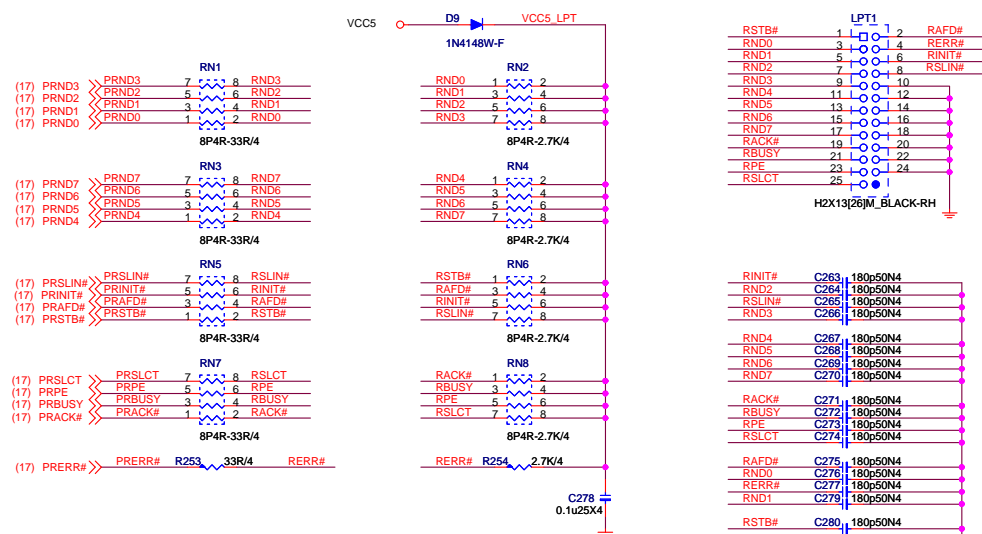


## SERIAL PORT 2

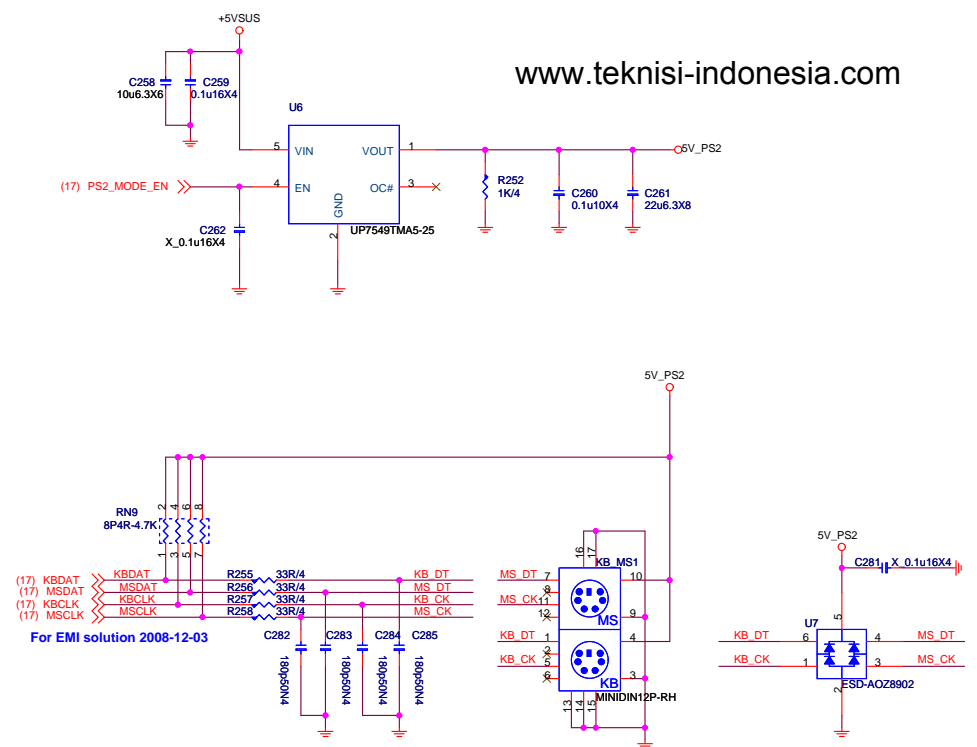


No stuff 2015.7.20

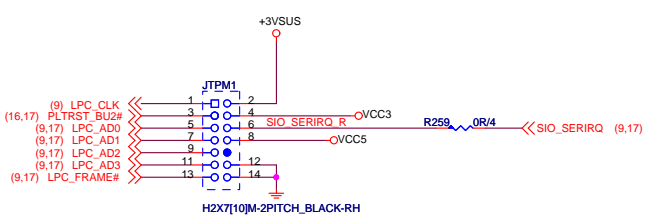
## PARALLAL PORT



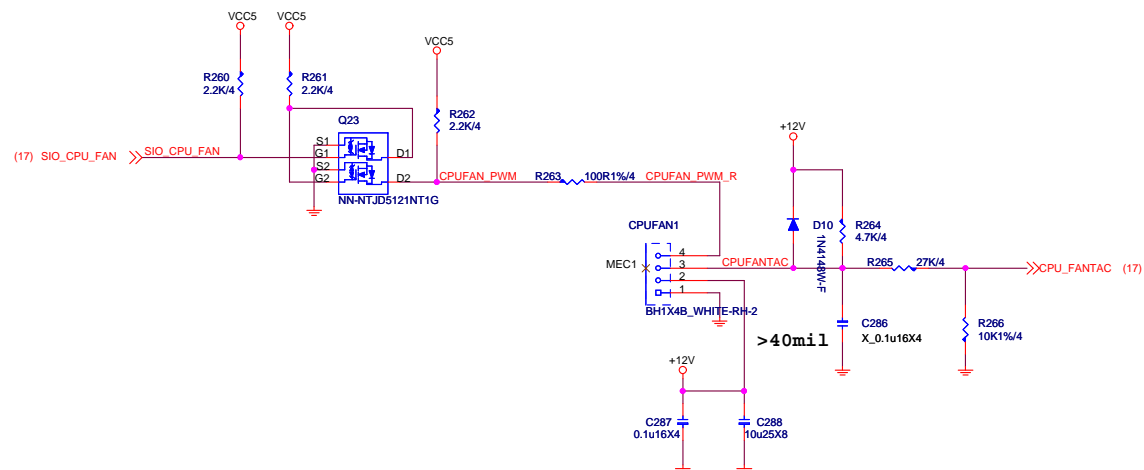
## PS2 KEYBOARD & MOUSE CONNECTOR



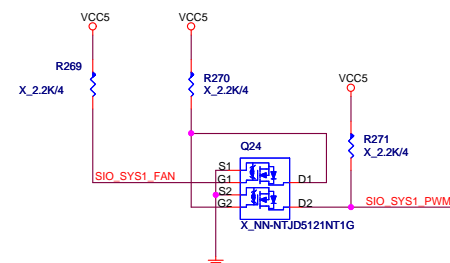
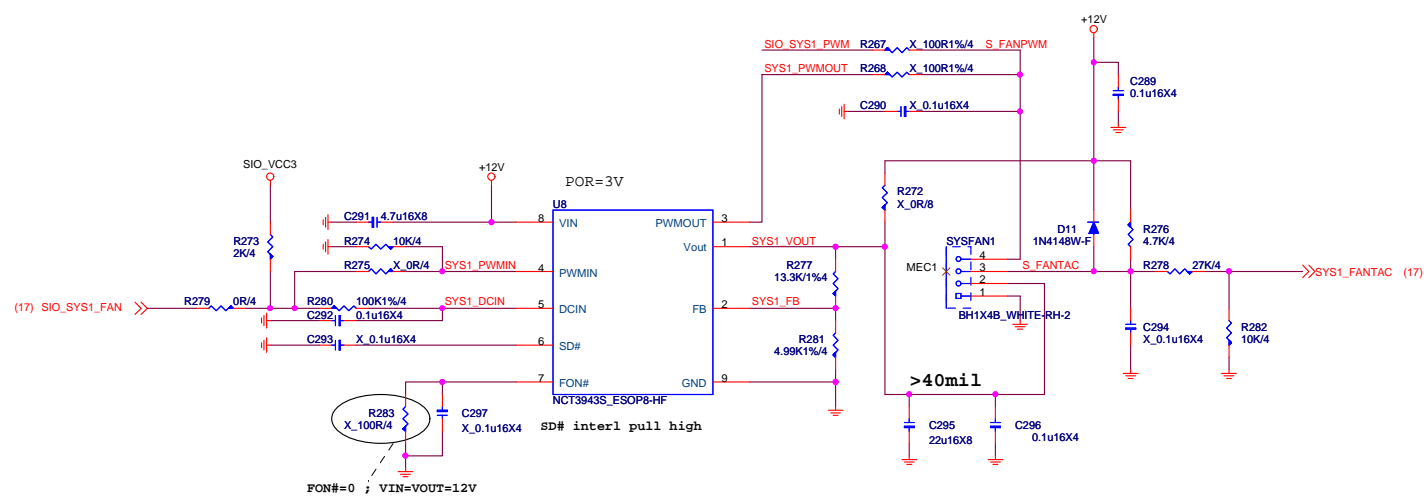
## TPM/JLPC



## CPUFAN

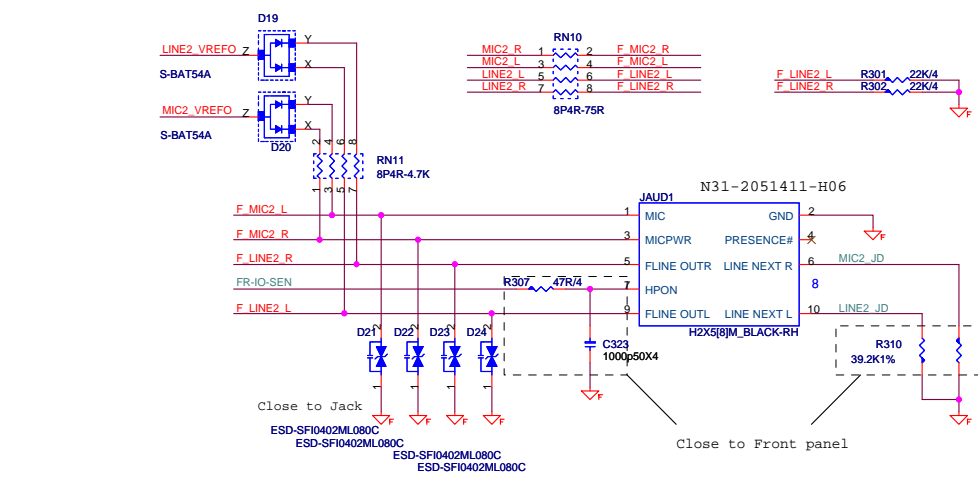
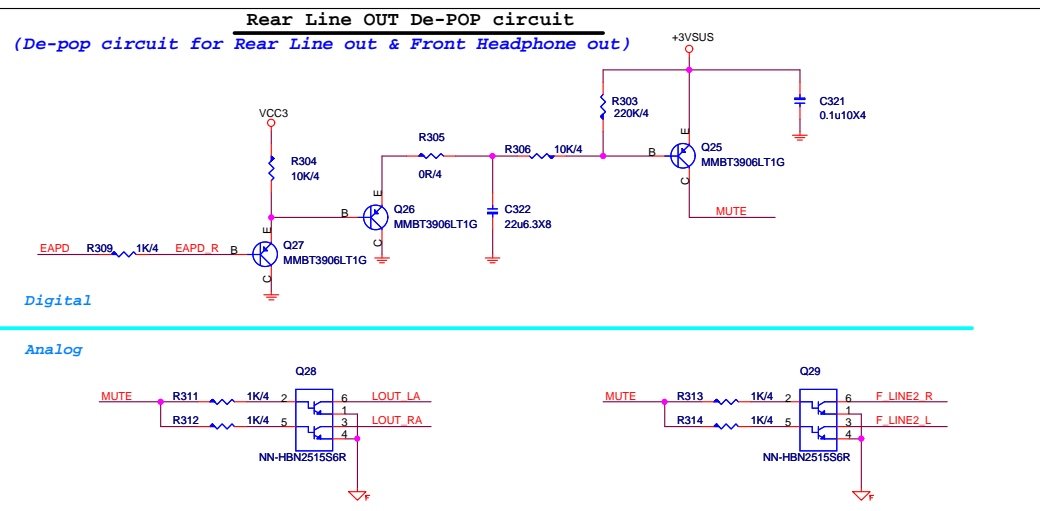
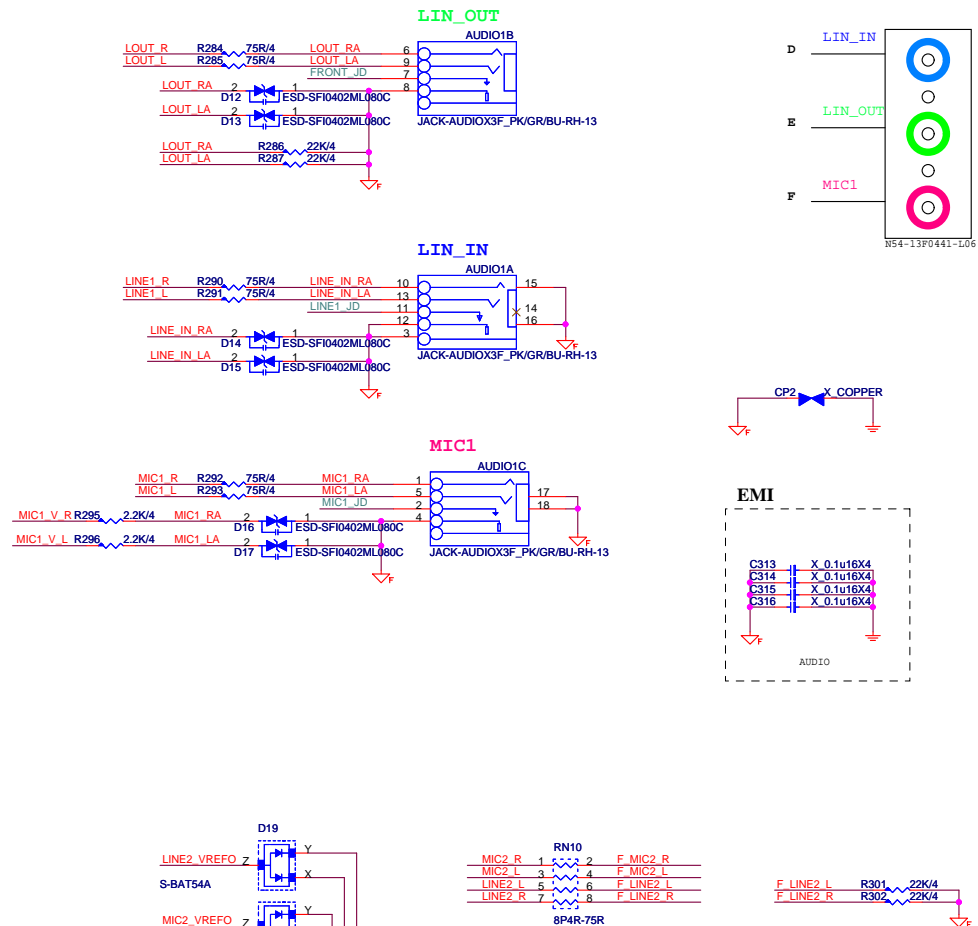
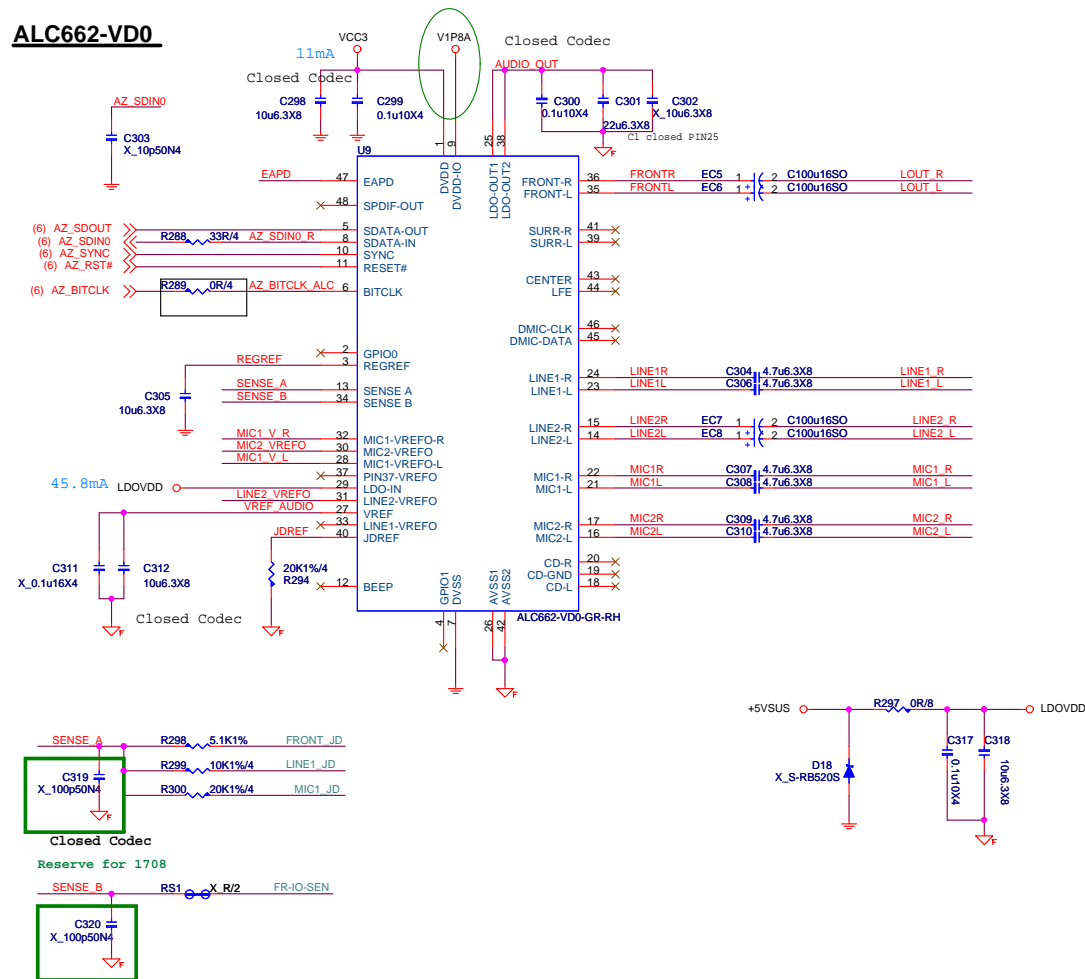


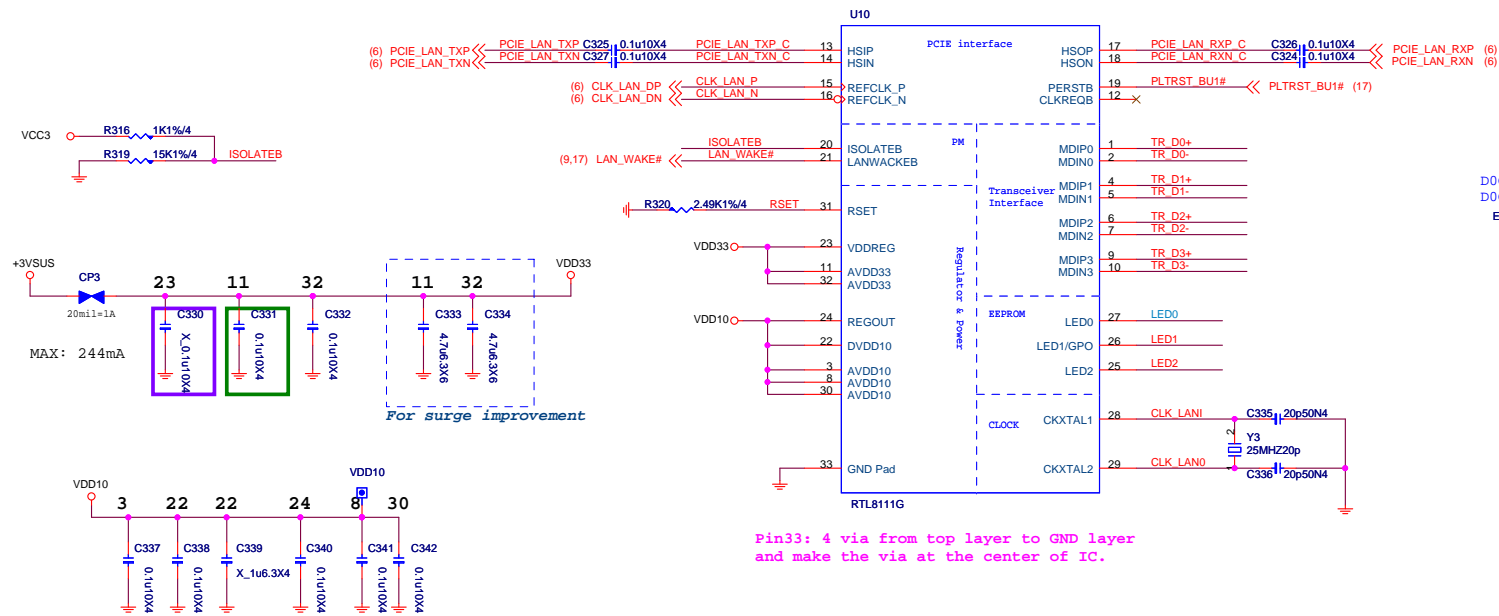
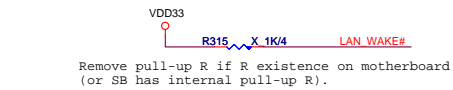
## SYSFAN



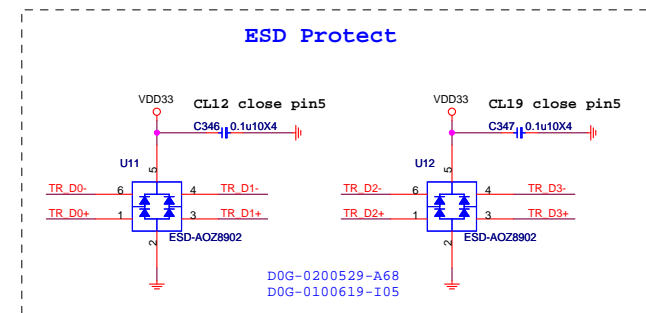
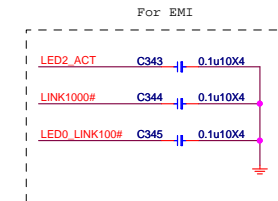
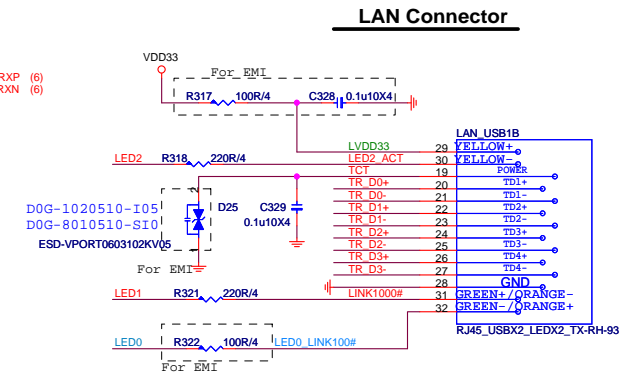
SYSFAN\_PWR\_OFF  
 SIO control  
 Close SIO\_SYS1\_FAN Vout=0

**ALC662-VD0**





Pin33: 4 via from top layer to GND layer and make the via at the center of IC.

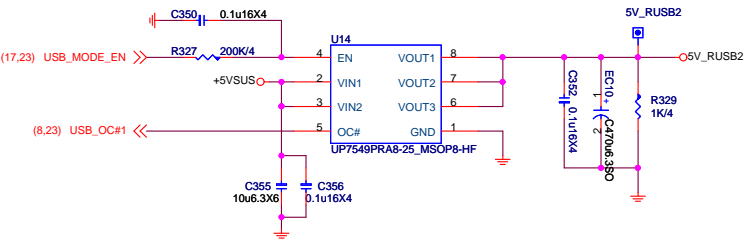
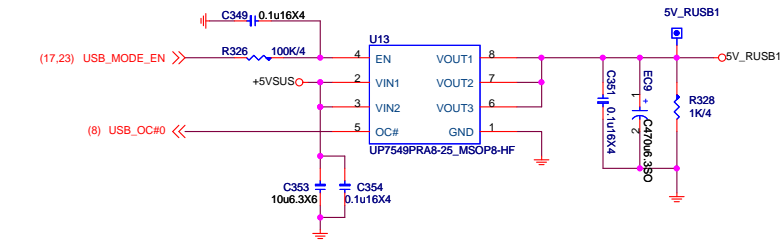


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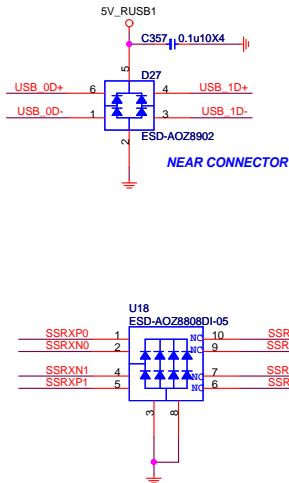
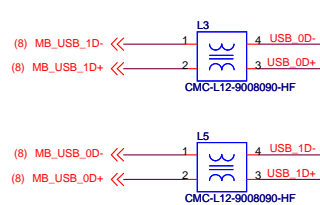
## 8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

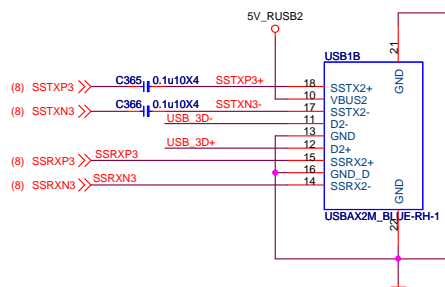
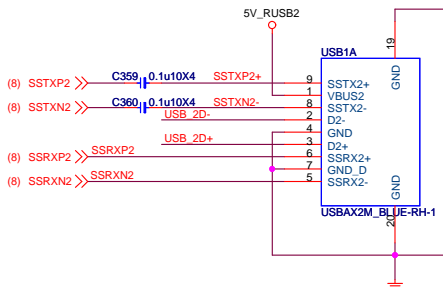
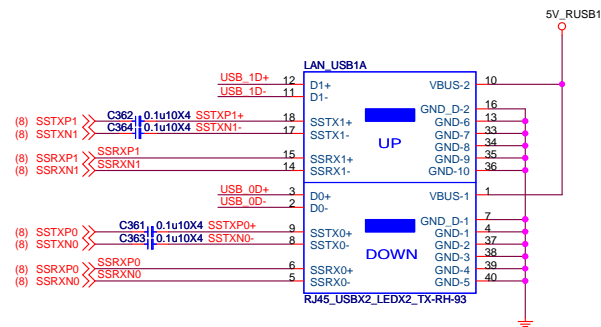
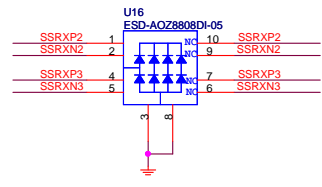
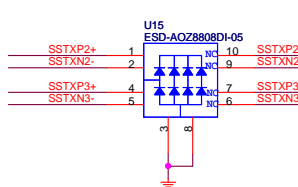
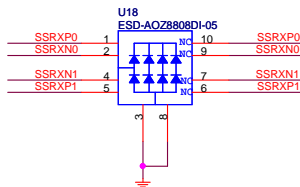
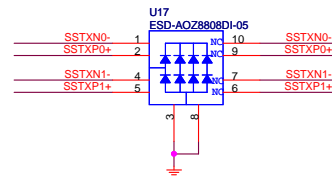
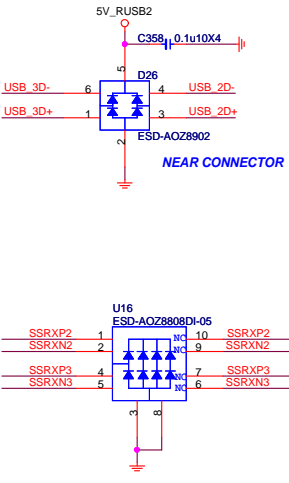
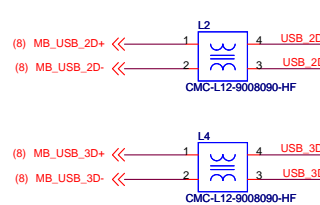
USB POWER: UP7549PRA8-25



Rear USB PORT 0,1



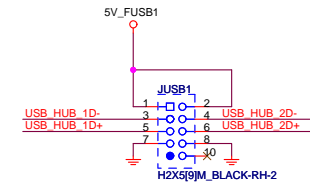
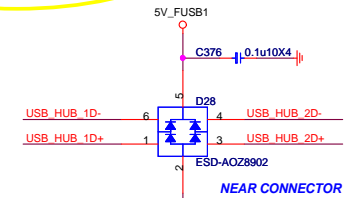
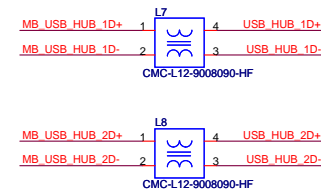
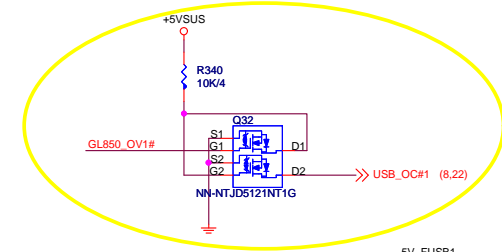
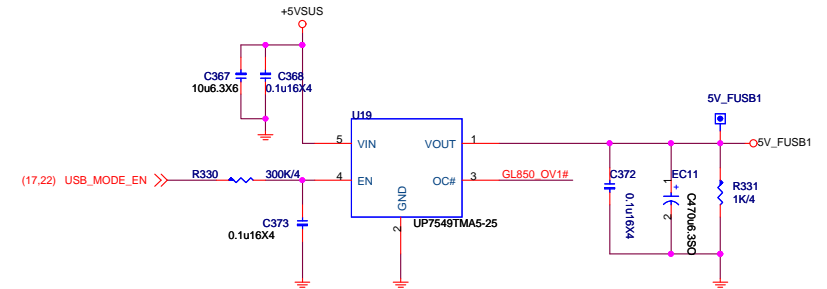
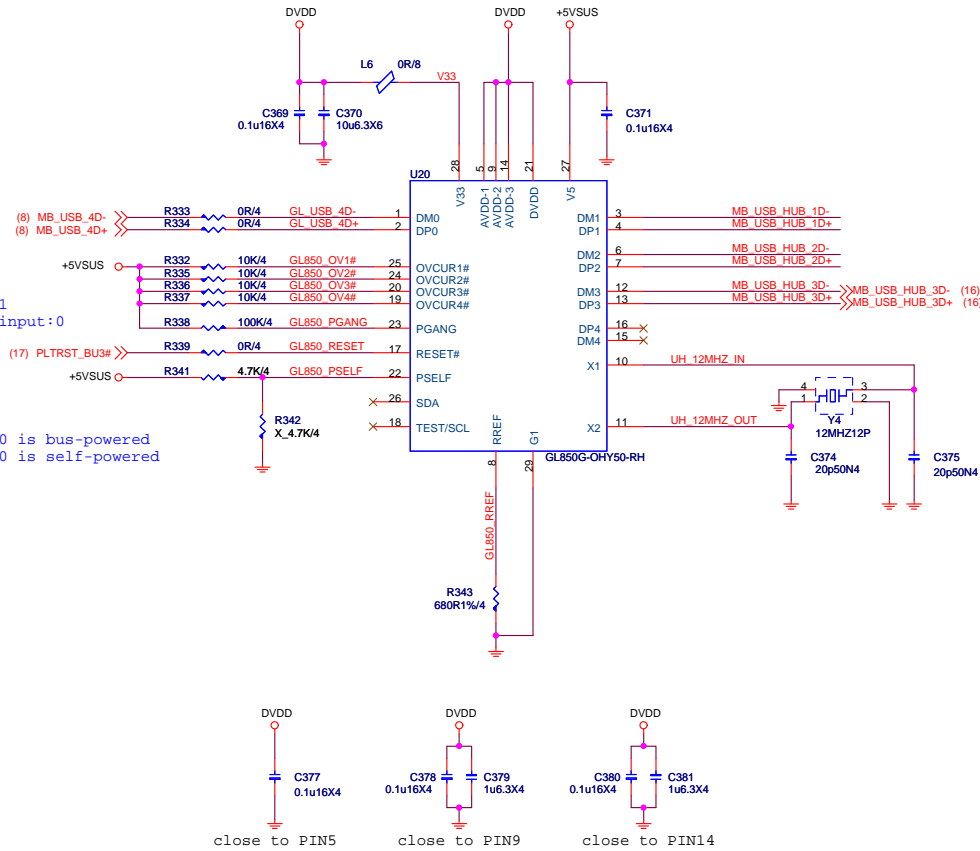
Rear USB PORT 2,3



# USB HUB

PIN23  
Gang input:1  
Individual input:0

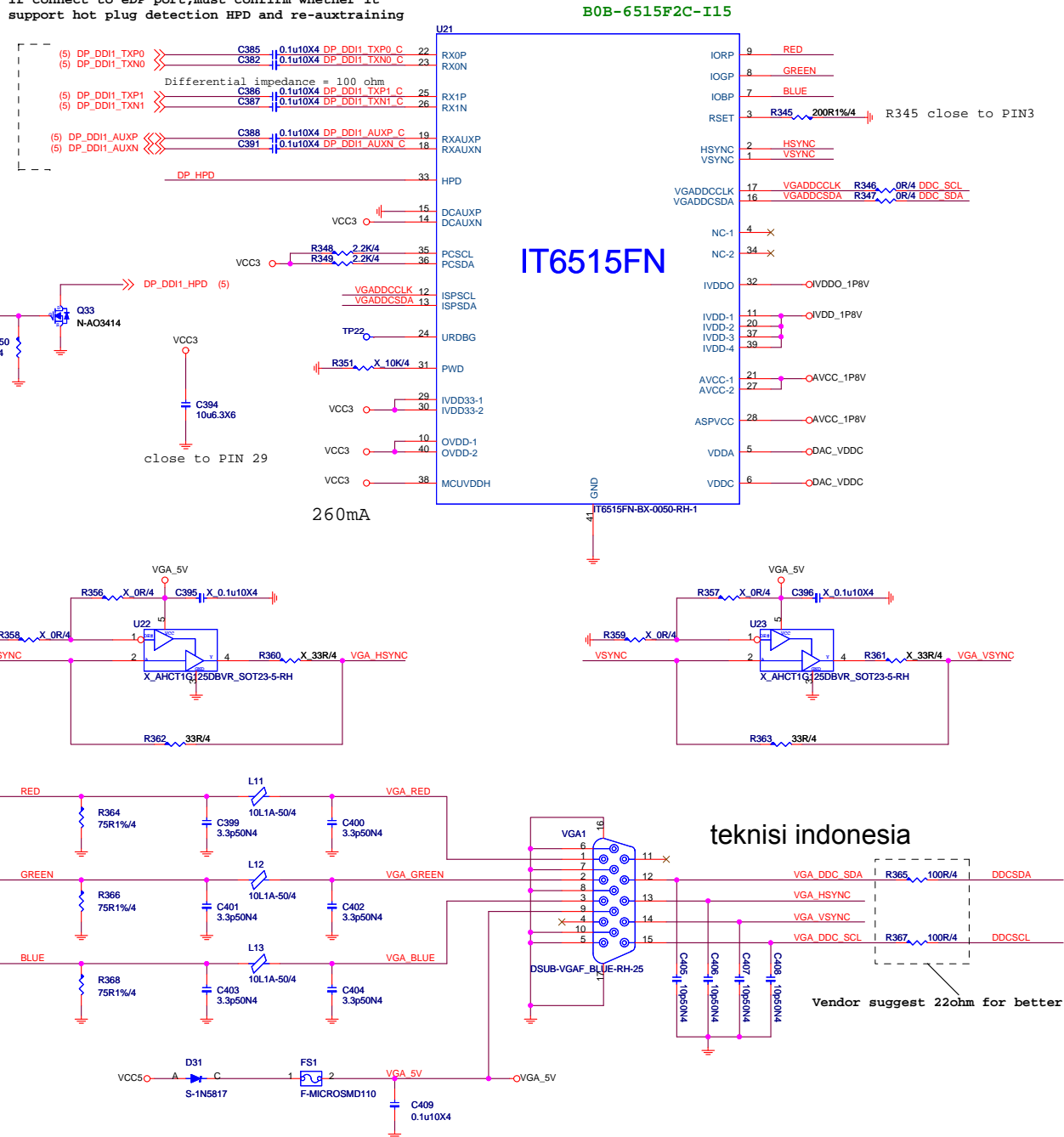
PIN22  
0: GL850G-50 is bus-powered  
1: GL850G-50 is self-powered



## D-Sub

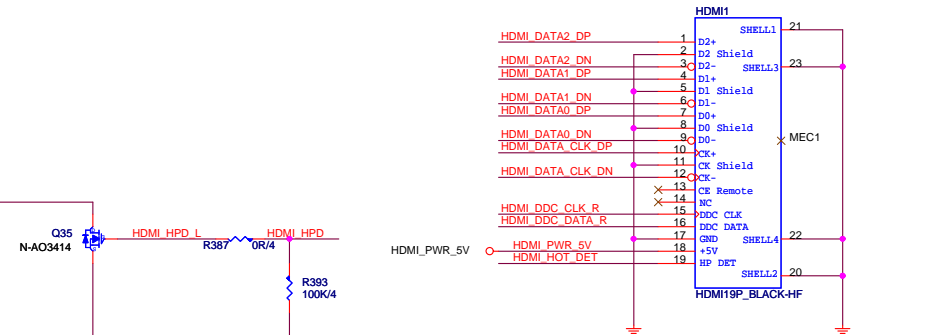
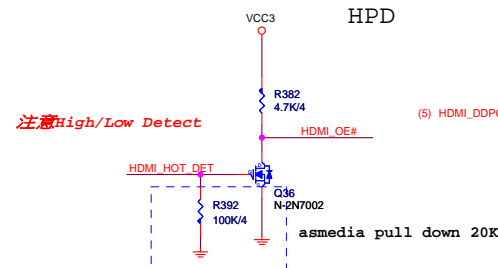
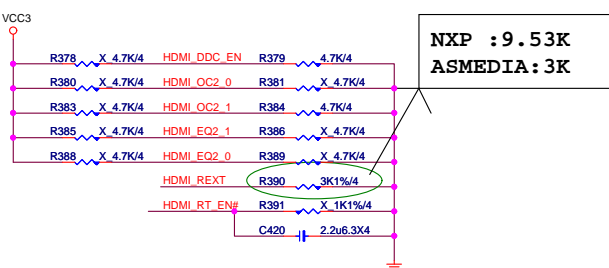
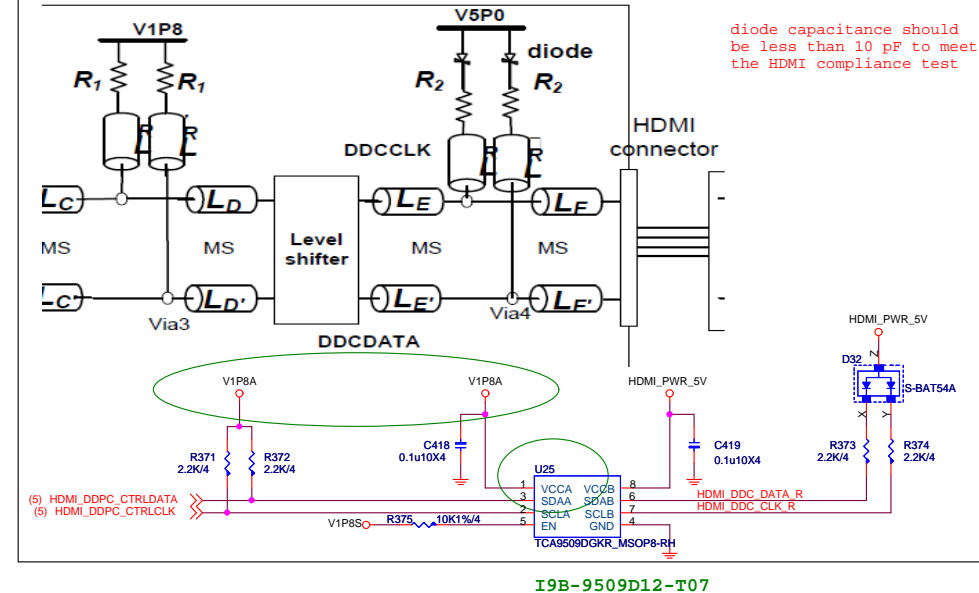
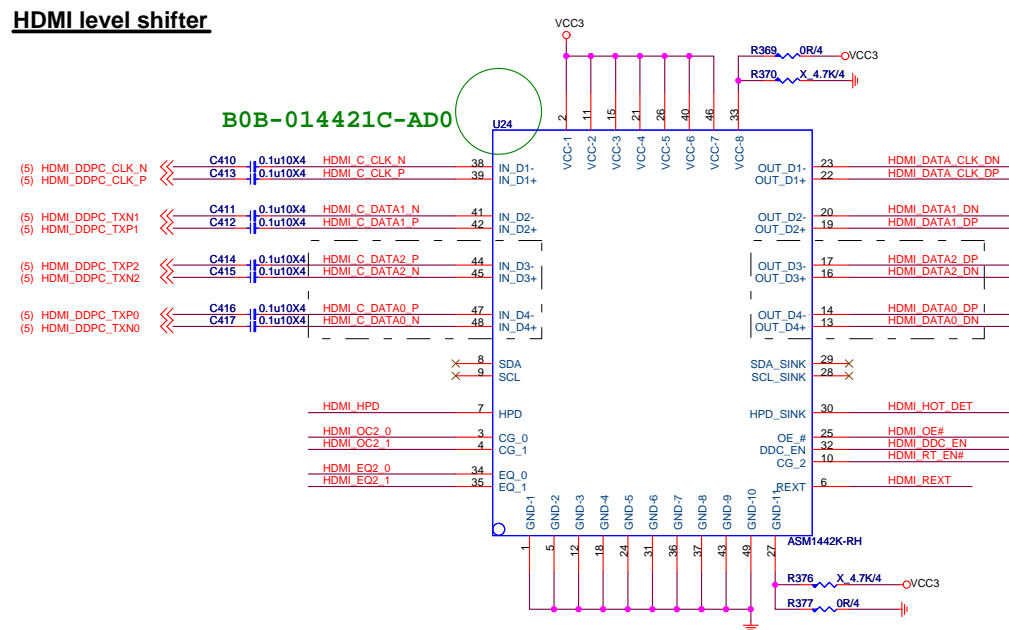
### Note:

If connect to eDP port, must confirm whether it support hot plug detection HPD and re-auxtraining



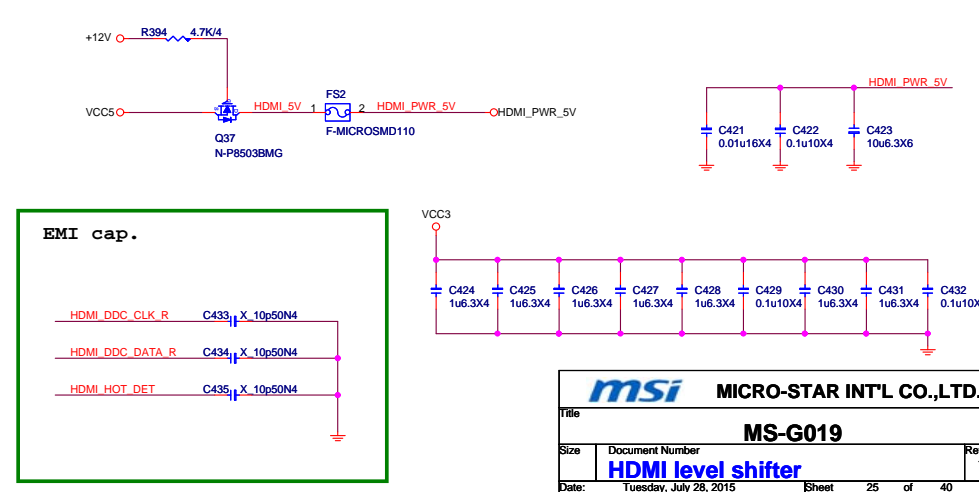
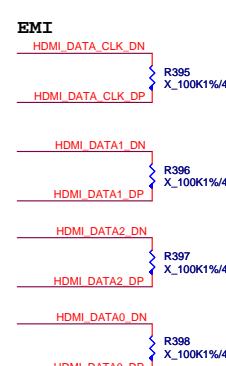


### HDMI level shifter

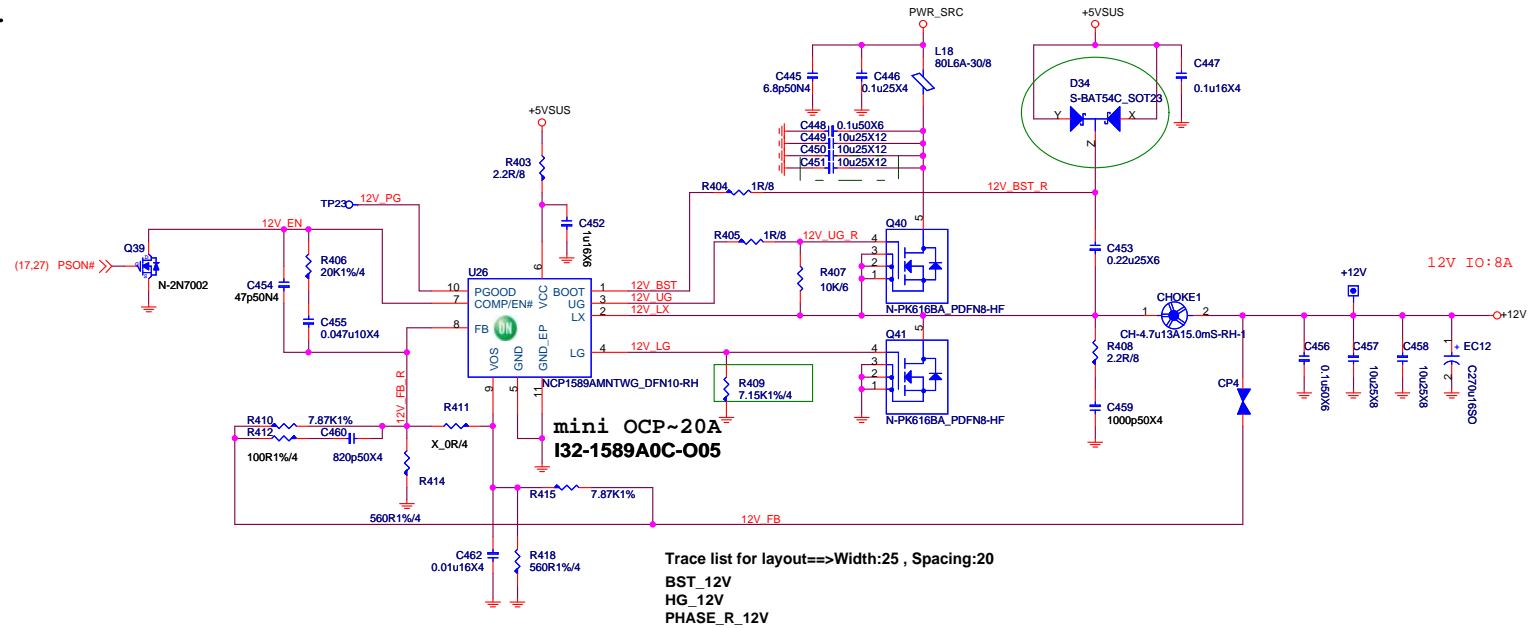


	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm
HPD_SINK	disable	enable	internal pull-down at ~200K ohm 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm
REXT			analog current

DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off



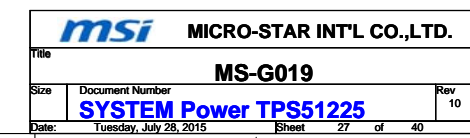
## +12V POWER



Trace list for layout==>Width:25 , Spacing:20  
BST\_12V  
HG\_12V  
PHASE\_R\_12V

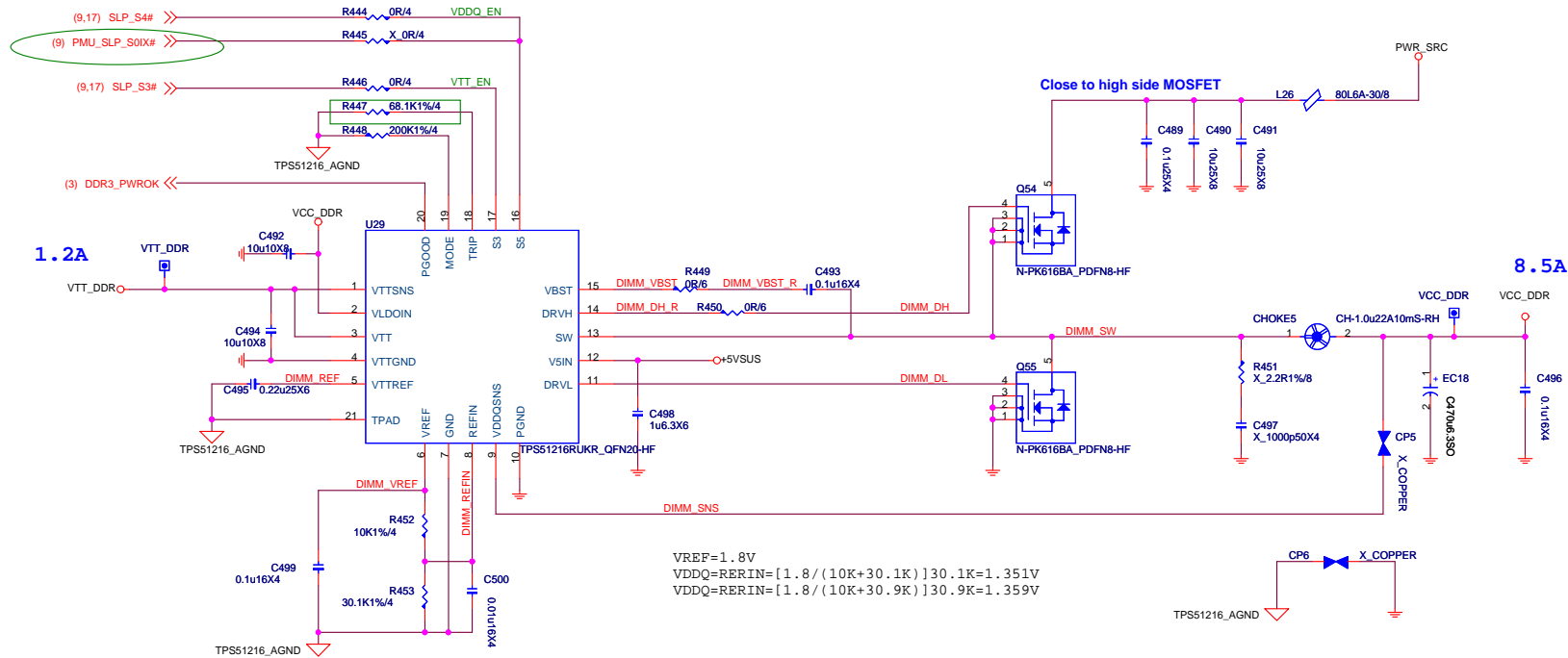
## +5VSUS/+3VSUS/VCC5/VCC3

EN1	EN2	VREG5	VREG3	CH1 (5Vout)	CH2 (3.3Vout)	VCLK	PGOOD
OFF	OFF	ON	ON	OFF	OFF	OFF	Low
ON	OFF	ON	ON	ON	OFF	ON	Low
OFF	ON	ON	ON	OFF	ON	OFF	Low
ON	ON	ON	ON	ON	ON	ON	High

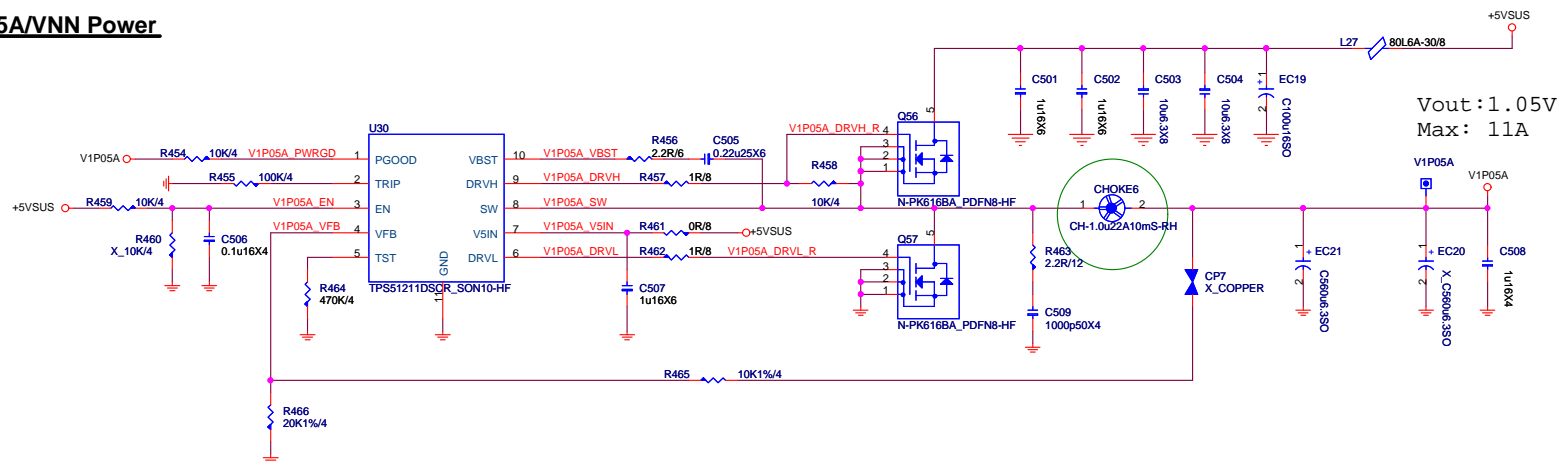


VCC\_DDR/VTT\_DDR POWER

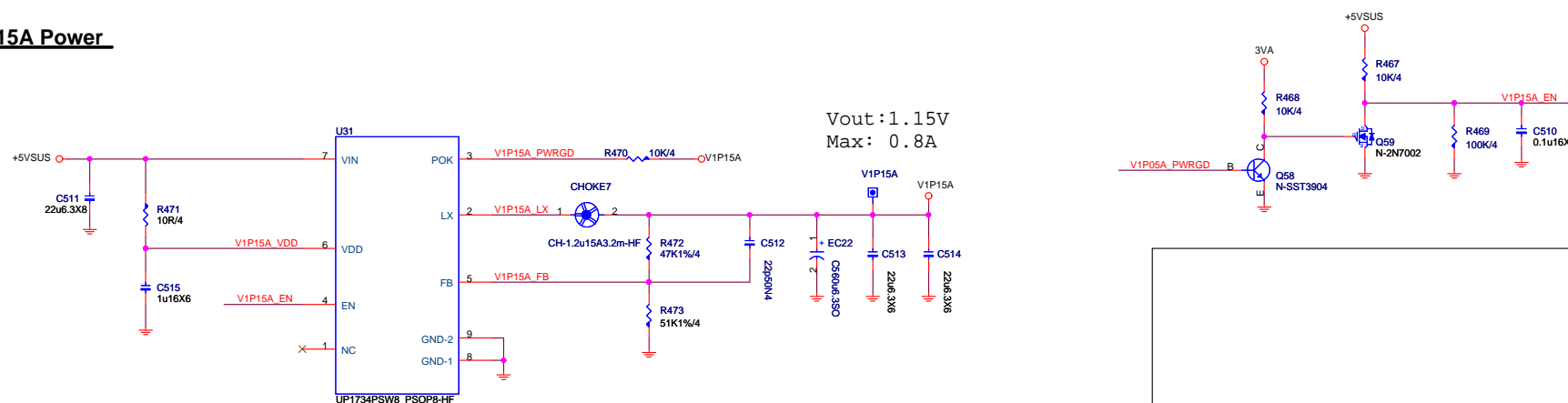
S3/S5 Power State Control						
STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)



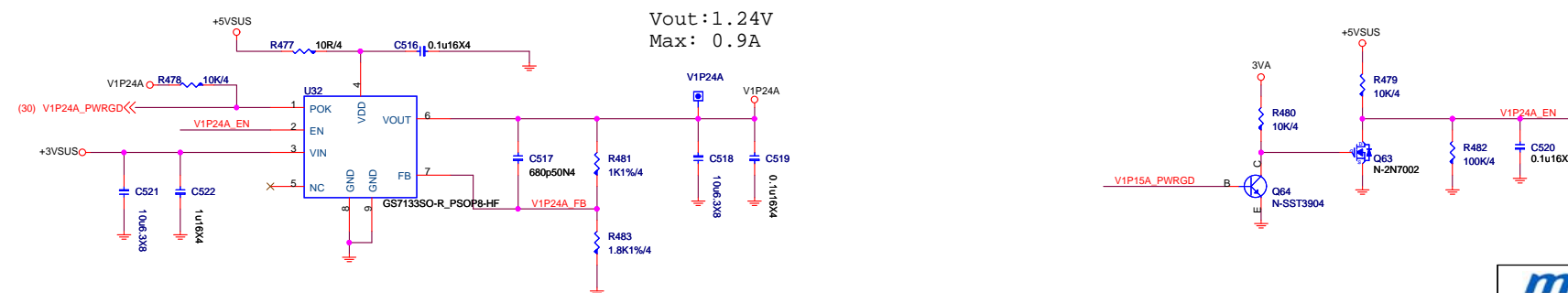
### V1P05A/VNN Power



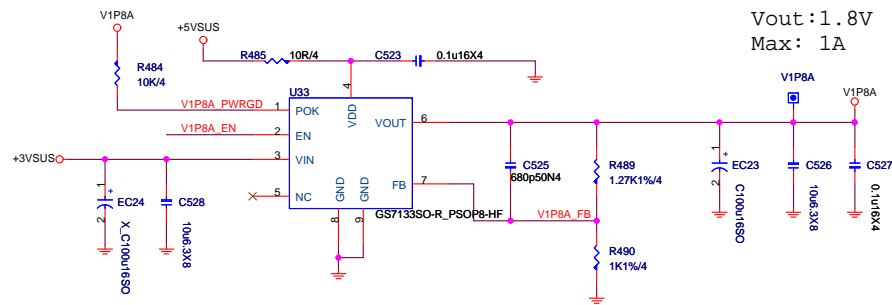
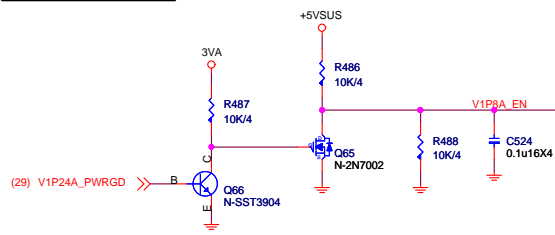
### V1P15A Power



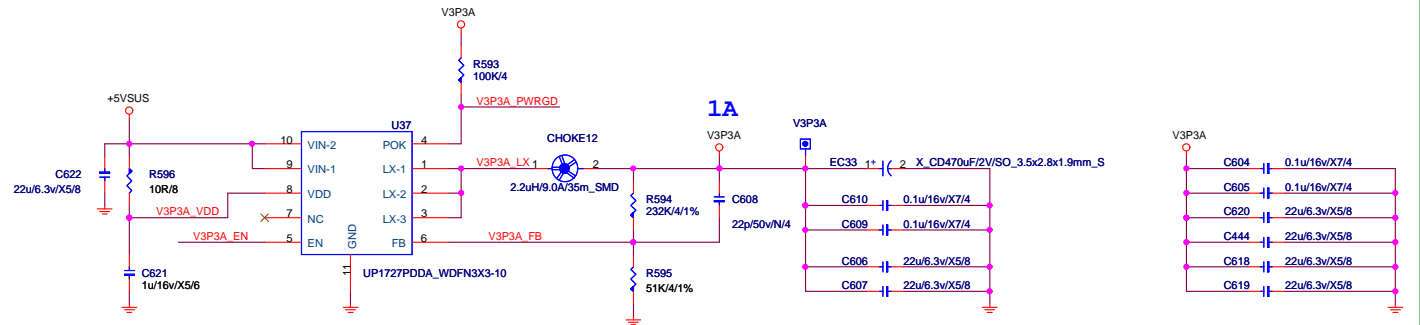
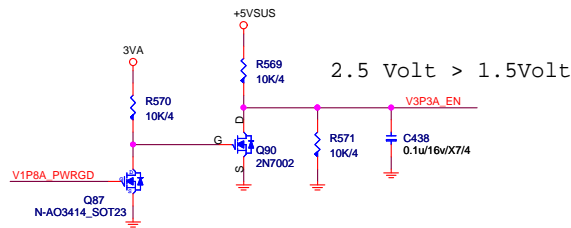
### V1P24A POWER



## V1P8A POWER



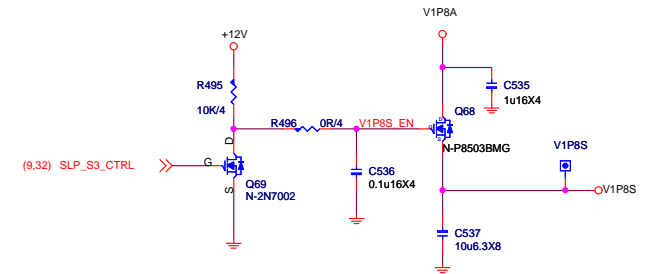
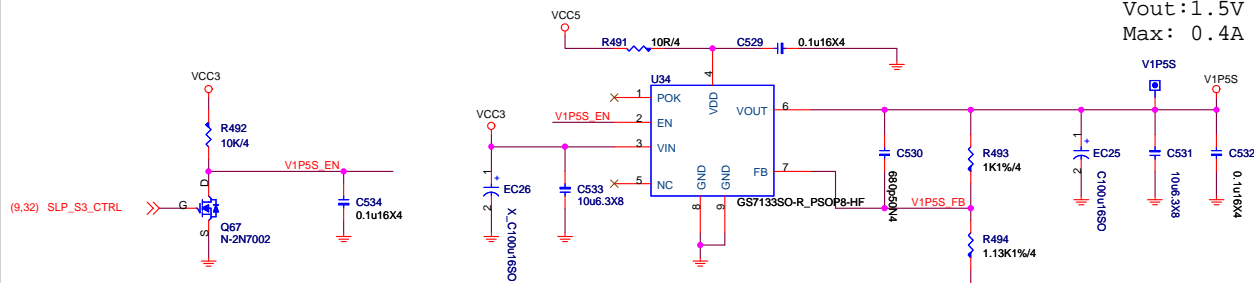
## V3P3A POWER



## V1P5S Power

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## V1P8S Power



## BRASWELL - VCORE ( SVID ADDRESS-00h )

VCORE\_VBOOT/ADDR

VBOOT=1V  
ADDR=00h

R529  
0R/4

VCORE\_IMAX

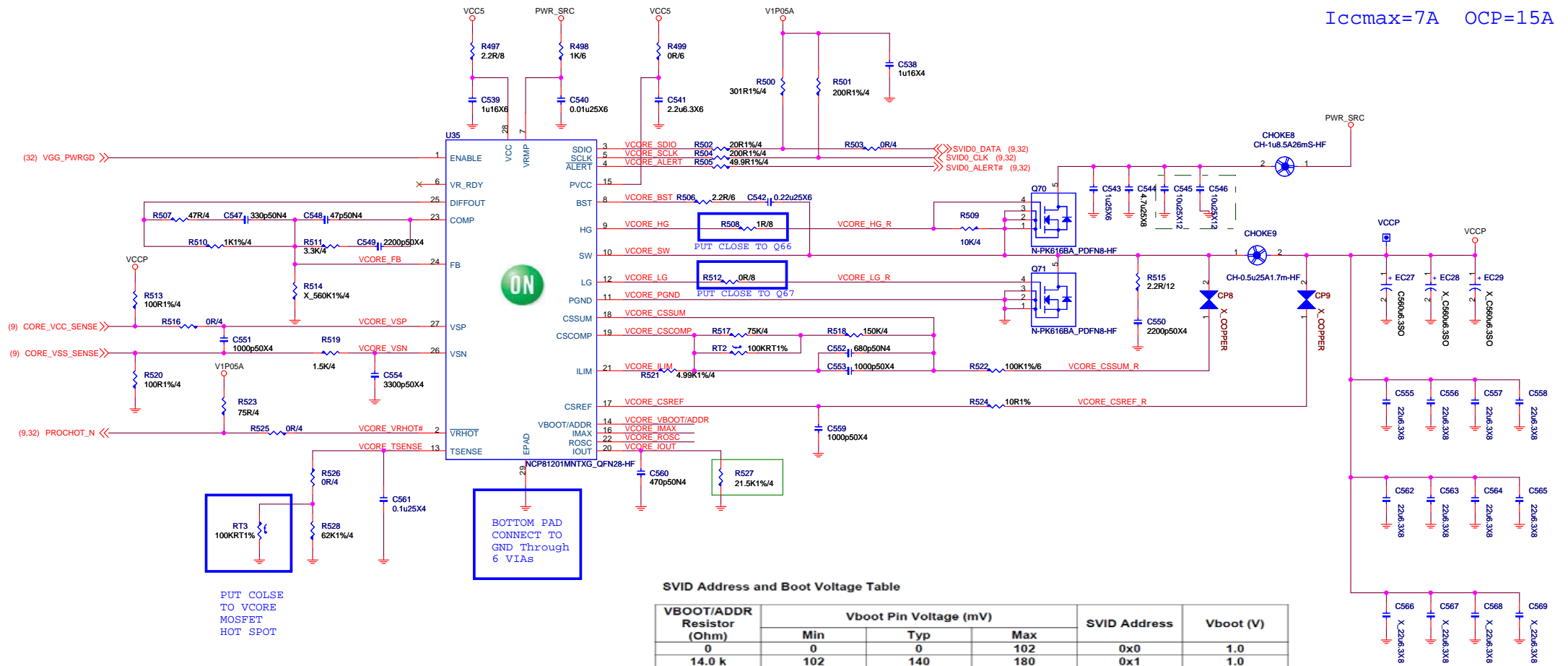
Imax=7A

R530  
24KR1%/4

VCORE\_ROSC

Frequency=1400Khz

R531  
24KR1%/4

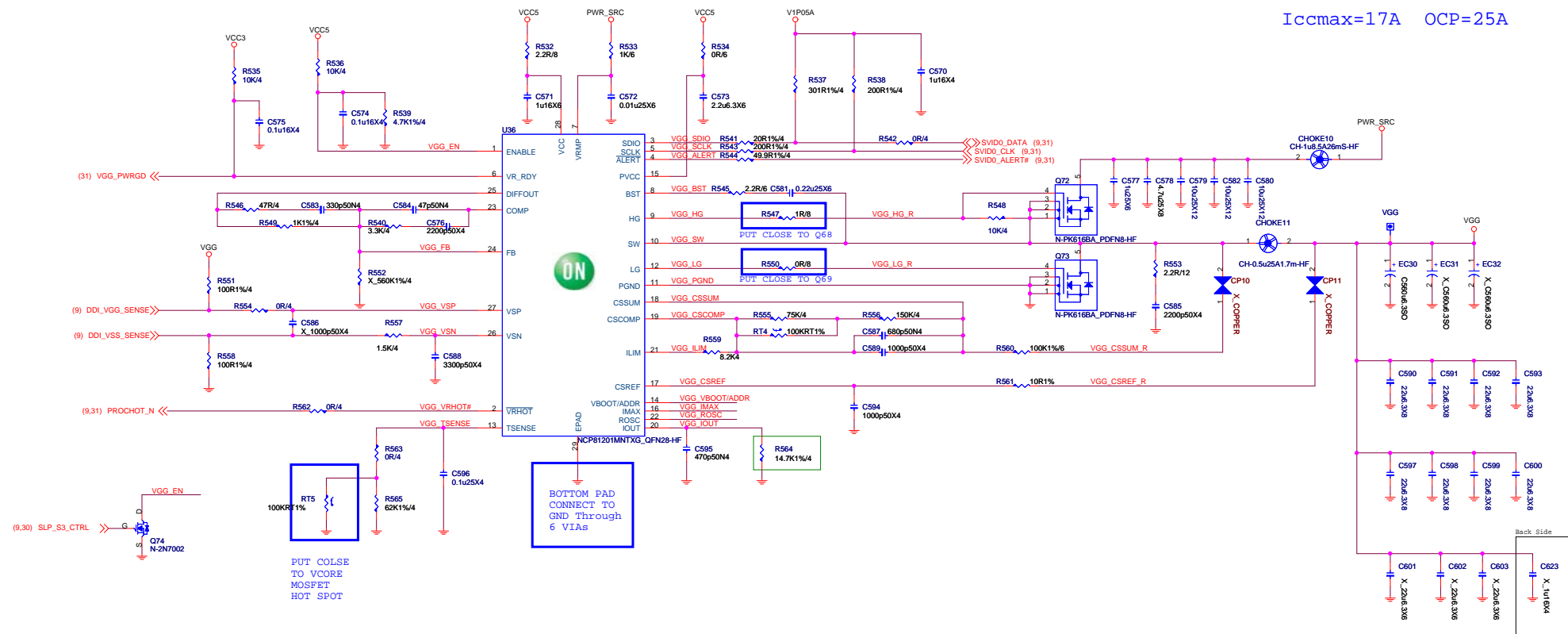


VBOOT/ADDR Resistor (Ohm)	Vboot Pin Voltage (mV)			SVID Address	Vboot (V)
	Min	Typ	Max		
0	0	0	102	0x0	1.0
14.0 k	102	140	180	0x1	1.0
22.1 k	180	219	258	0x2	1.0
30.1 k	258	301	344	0x3	1.0
39.2 k	344	391	438	0x4	1.0
48.7 k	438	484	531	0x5	1.0
57.6 k	531	578	625	0x6	1.0
68.1 k	625	676	727	0x7	1.0
78.7 k	727	781	836	0x8	1.1
88.7 k	836	894	953	0x0	1.1
100 k	953	1007	1062	0x1	1.1
113 k	1062	1125	1188	0x2	1.1
124 k	1188	1250	1312	0x3	1.1
137 k	1312	1378	1445	0x4	1.1
150 k	1445	1511	1578	0x5	1.1
165 k	1578	1648	1719	0x6	1.1
178 k	1719	1789	1859	0x7	1.1
196 k	1859	1950	-	0x8	1.1

### VGG Power

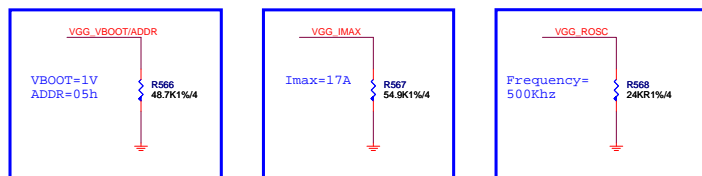
## BRASWELL - VGG ( SVID ADDRESS-05h )

Iccmax=17A    OCP=25A



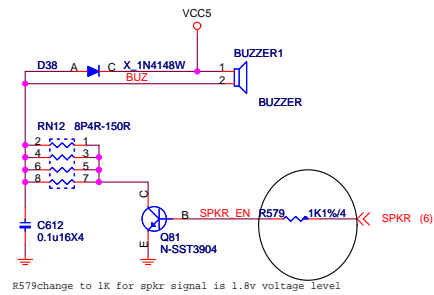
### SVID Address and Boot Voltage Table

VBOOT/ADDR Resistor (Ohm)	Vboot Pin Voltage (mV)			SVID Address	Vboot (V)
	Min	Typ	Max		
0	0	0	102	0x0	1.0
14.0 k	102	140	180	0x1	1.0
22.1 k	180	219	258	0x2	1.0
30.1 k	258	301	344	0x3	1.0
39.2 k	344	391	438	0x4	1.0
48.7 k	438	484	531	0x5	1.0
57.6 k	531	578	625	0x6	1.0
68.1 k	625	676	727	0x7	1.0
78.7 k	727	781	836	0x8	1.1
88.7 k	836	894	953	0x0	1.1
100 k	953	1007	1062	0x1	1.1
113 k	1062	1125	1188	0x2	1.1
124 k	1188	1250	1312	0x3	1.1
137 k	1312	1378	1445	0x4	1.1
150 k	1445	1511	1578	0x5	1.1
165 k	1578	1648	1719	0x6	1.1
178 k	1719	1789	1859	0x7	1.1
196 k	1859	1950		0x8	1.1

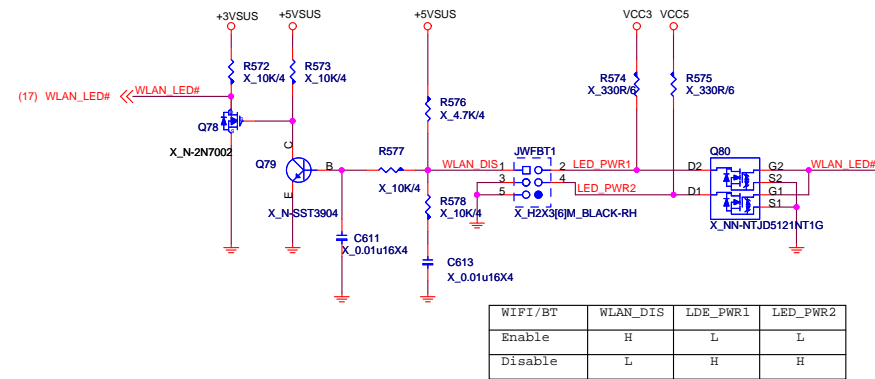




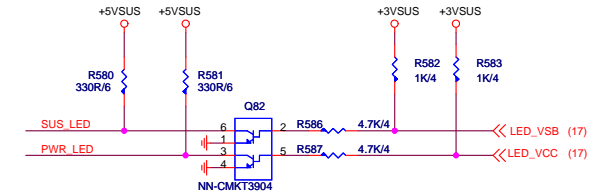
### Speaker Pin Header



## WIFI & BT LED



### Power LED



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### FRONT PANNEL

CRB Pull up VAP8A.  
Follow EDS update, it is vlp8s powered.

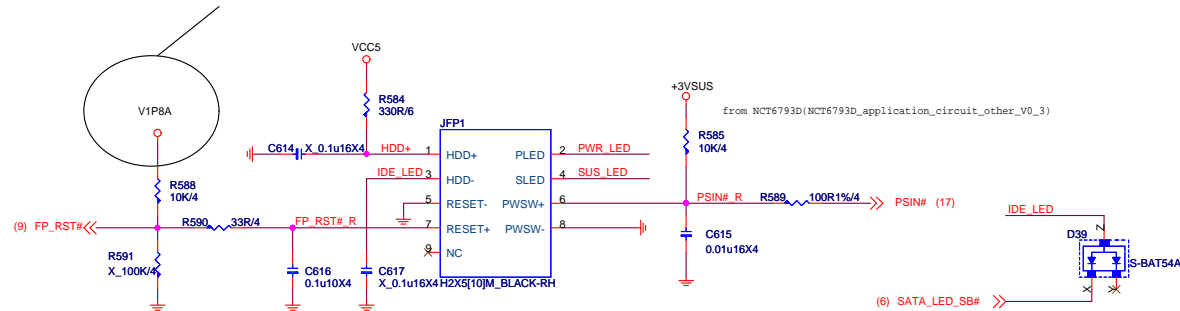
**EMI**

TABLE1  
*Label*  
BIOS  
BIOS\_LABEL

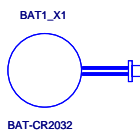
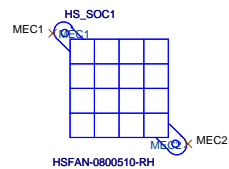
CPU1  
*CPU*  
SOC-OPT

TABLE2  
*Label*  
HDMI  
HDMI\_LABEL

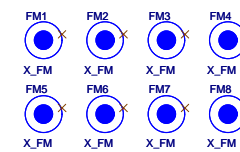
## Simulation



## SOC



## Optical Fiducial Marks-120



## Mounting Holes

